Linko Semiconductor Co., Ltd.

LKS32MC08X with built-in 6N driver Datasheet

1 Overview

1.1 Function

LKS32MC084D/086 is a 32-bit MCU targeting motor control applications. With the three-phase full-bridge bootstrap gate driver, it can directly drive six N-channel MOSFETs.

Features

- 96MHz 32-bit RISC core
- Customized instruction set DSP for motor control
- Ultra low power sleep mode, 10uA sleep current with MCU low low power consumption
- Three-phase full-bridge bootstrap gate driver
- Industrial temperature range
- High ESD and group pulse reliability

- **Memory**
  - 64/32kB Flash with optional encryption to prevent hex theft
  - 8kB RAM
- **Operating Conditions**
  - Dual power supply. The MCU is powered by 2.2V ~ 5.5V voltage(B-version chip is powered by 3.0V~5.5V), with an integrated internal LDO for the digital circuit. Drive module power supply please refer to Chapter 22.
  - Operating Conditions: -40~105℃
- **Clock**
  - 4MHz built-in high-precision RC oscillator, with an accuracy of ± 1% at -40 ~ 105 ℃
  - 32KHz built-in low-speed clock for low-power mode
  - Operating on an external 4MHz crystal is available
  - Internal PLL up to 96 MHz
- **Peripheral Modules**
  - Two UARTs
  - One SPI, support master-slave mode
  - One IIC, support master-slave mode
  - One CAN-bus (084D without CAN), recommended to use external crystal as reference clock
  - Two 16-bit standard timers (TIM), support capture and edge-aligned PWM function
  - Two 32-bit standard timers (TIM), support capture and edge-aligned PWM function; support orthogonal code input, CW/CCW input, and pulse&symbol input
  - Motor control PWM module, supports 8 channels/4 pairs of PWM waveform output, independent dead-band control
  - Hall signal interface with speed measurement and debouncing function

  - Hardware watchdog
  - 4 Groups of 16bit GPIO at the most. P0.0/P0.1/P1.0/P1.1 could be used as wake-up source。
    P0.15 ~ P0.0 could be used as external IRQ source
- **Analog Modules**
  - 12bit SAR ADC, simultaneous double sampling, 3Msps sampling and conversion rate, up to 13 analog signal channels
  - Four operational amplifiers. Differential PGA mode is available.
  - Two comparators. Hysteresis mode is available.
  - 12bit digital-to-analog converter (DAC)
  - ± 2 °C built-in temperature sensor
  - 1.2V 0.8% built-in linear regulator
  - Low-power LDO and power monitoring circuit
  - RC oscillator with high precision and low temperature drift
  - Crystal oscillator circuits

1.2 Performance Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 4 channels high-speed OPAs and 2 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed hight current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Three-phase full-bridge bootstrap gate driver is integrated;
- Supports IEC/UL60730 functional safety certification;

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Conventions

LKS32 MC 080 R 8 T 8 XX (X)

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

080/081/082/ 083/085/088	= 2.2~5.5V,1 ADC,4 PGA,DSP
084D/086	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver
087(A)	= 2.2~5.5V,1 ADC,2 PGA
087C	= 2.2~5.5V,1 ADC,2 PGA, CAN
087D/087E	= 7.5~28V, 1 ADC,2 PGA,3P3N Driver
089	= 2.2~5.5V,1 ADC,2 PGA
089XL	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver,LIN

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Options

TR	= Tape and reel packing
P	= Engineering Samples

Version

X	= Version, B~Z

Fig. 1-1 Naming Conventions of Linko Components

1.4 Resource Diagram

The resources of LKS32MC086N8Q8(B) are shown in the following figure. For other models, please refer to the chip selection guide.

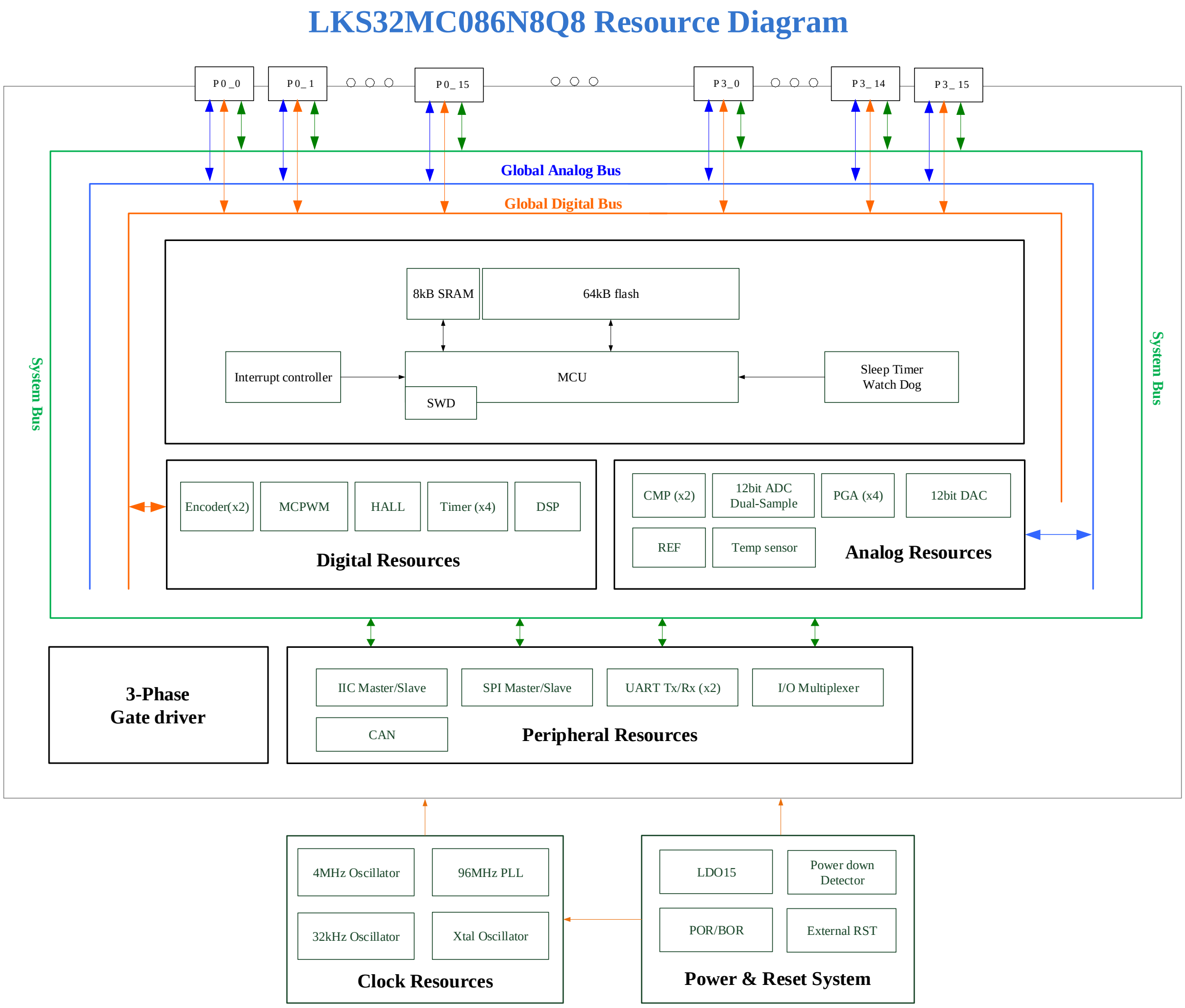

Fig. 1-2 LKS32MC086N8Q8(B) Resource Diagram

1.5 FOC System Example

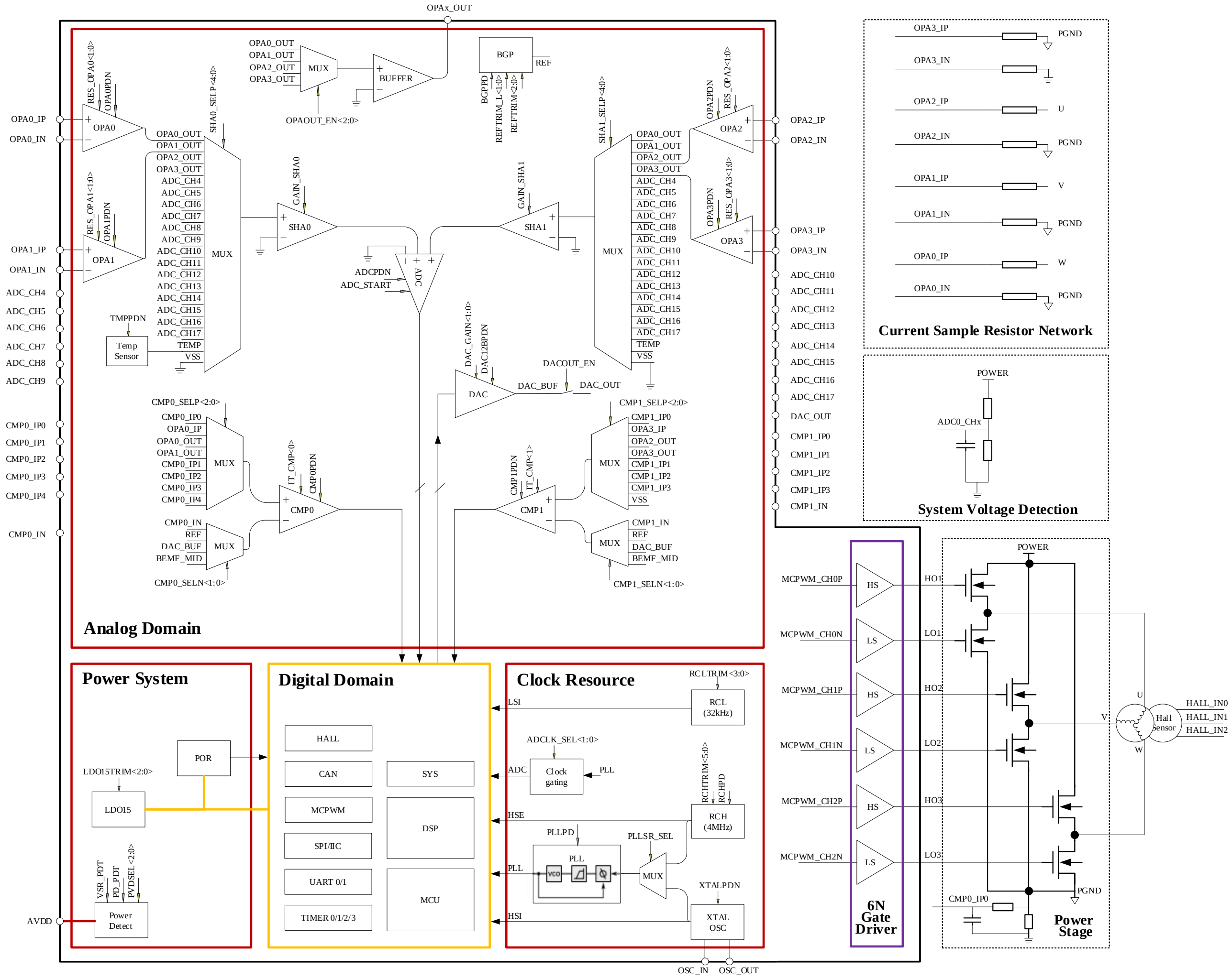

Fig. 1-3 LKS32MC086N8Q8(B) Simplified Schematic of FOC System

2 Device Selection Guide

Table 2-1 LKS08x family device selection guide

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC080R8T8(B)	96	64	8	13	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						LQFP64
LKS32MC081C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC082K8Q8(B)	96	64	8	8	12BITx1	2	6	3	3	1	1	2		Yes	Yes							QFN5*5 32L-0.75
LKS32MC083C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						TQFP48
LKS32MC084DF6Q8	96	32	8	11	12BITx1	2	7	3	3	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20*1	200		QFN5*5 40L-0.75
LKS32AT085C8Q9	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						QFN6*6 48L-0.55
LKS32AT086N8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC086N8Q8	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC087M6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087AM6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087CM8S8(B)	96	64	8	5	12BITx1	2	6	2	3			1	Yes	Yes	Yes							SSOP24L
LKS32MC087DM6S8	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO*2	SSOP24L
LKS32MC087EM6S8	96	32	8	5	12BITx1	2	7	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO	SSOP24L
LKS32MC088C6T8(B)	96	32	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC088KU8Q8	96	64	8	8	12BITx1	2	7	3	3	1	1	2	Yes	Yes	Yes	Yes	6N	+0.45/-1	4.5~20	600	5V LDO	QFN43L
LKS32MC088K22U8Q8	96	64	8	8	12BITx1	2	7	3	3	1	1	2	Yes	Yes	Yes	Yes	6N	+0.45/-1	4.5~20	600	5V LDO	QFN43L
LKS32AT089XLN8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200	5V LDO	QFN6*6 52L-0.55

*1 : Some devices are divided into different versions due to the integration of multiple pre drives. The power supply voltage range of the pre drive is different. Please refer to the electrical performance parameters for details.

*2: Some devices are equipped with a 5V LDO, which is powered by 7.5~28V VCC and could supply 5V to MCU or peripheral devices. Please refer to Pin assignment table for more information.

3 Pin Assignment

3.1 Pin Assignment and Pin Function Description

3.1.1 Special Notes

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.
SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32MC084DF6Q8(B)

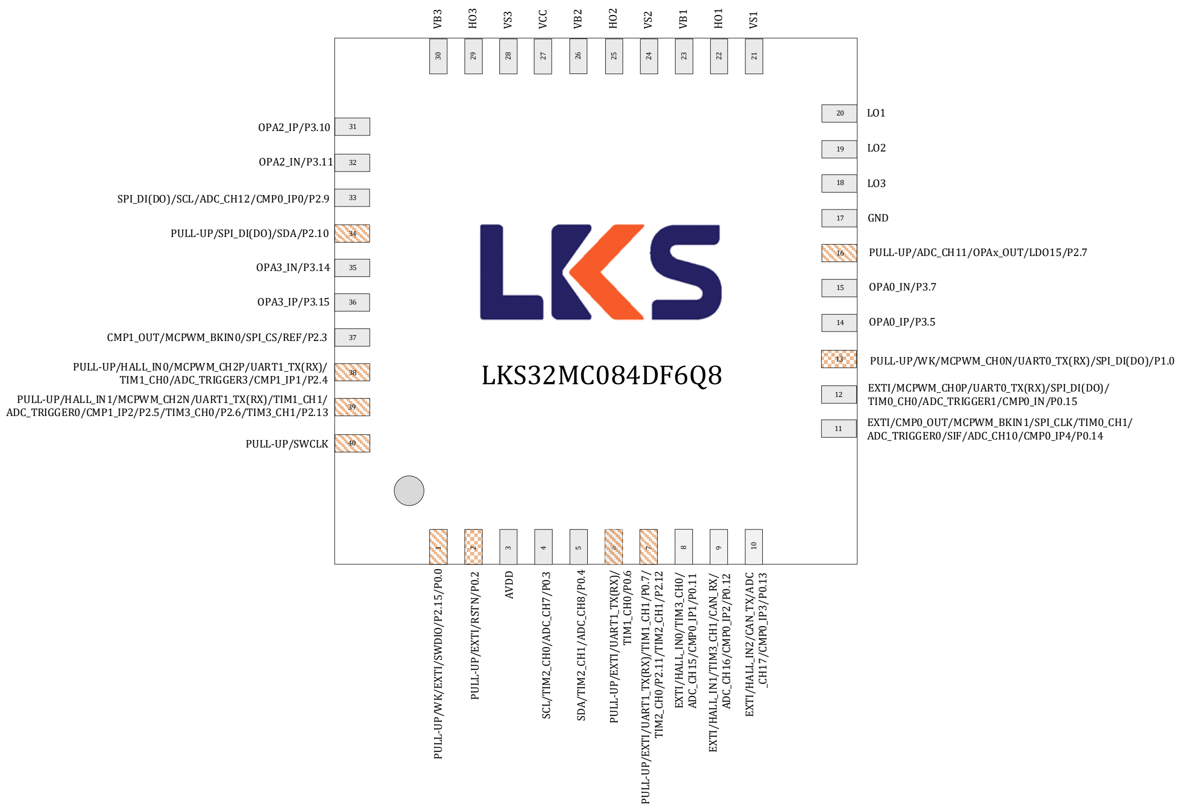

Fig. 3-1 LKS32MC084DF6Q8(B) Pin Assignment

Table 3-1 LKS32MC084DF6Q8(B) Pin Function Description

No.	Pin Name	Type	Pin Function Description
0	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
1	SWDIO/P2.15/P0.0	Input/Output	SWD data/P2.15/P0.0, with a 10k software-enabled built-in pull-up resistor. DAC output, P2.15 and P0.0 output cannot be used at the same time. While using the DAC output, P2.15 or P0.0 output, there must be a way to turn them off when SWD debugging or download is needed.
2	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF capacitor between RSTN and ground, RSTN has a 100k built-in pull-up resistor.
3	AVDD	Power	Chip power input, voltage range 2.2 ~ 5.5V(B-version chip is powered by 3.0V~5.5V). An off-chip decoupling capacitor of ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
4	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	IIC clock/Timer2 channel 0/ADC channel 7/P0.3
5	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	IIC data/Timer2 channel 1/ADC channel 8/P0.4
6	UART1_TX(RX)/TIM1_CH0/P0.6	Input/Output	UART1 TX(RX)/Timer1 channel 0/P0.6, with a 10k software-enabled built-in pull-up resistor.
7	UART1_TX(RX)/TIM1_CH1/P0.7	Input/Output	UART1 TX(RX)/Timer1 channel 1/P0.7, with a 10k software-enabled built-in pull-up resistor.
8	TIM2_CH0/P0.9/TIM2_CH1/P0.10/ HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP 1/P0.11	Input/Output	Timer2 channel 0/P0.9/ Timer2 channel 1/P0.10/ Hall sensor A phase input/Timer3 channel 0/ADC channel 15/positive input 1 for comparator 0/P0.11. P0.9, P0.10 and P0.11 are three independent IO connected together to this pin, so the output functions can't be used at the same time.
9	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP 2/P0.12	Input/Output	Hall sensor B-phase input/Timer3 channel 1/ADC channel 16/ positive input 2 for comparator 0/P0.12
10	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor C-phase input/ADC channel 17/ positive input 3 for comparator 0/P0.13
11	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM 0_CH1/ ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0. 14	Input/Output	Comparator 0 output/motor PWM breaking signal 1/SPI clock/Timer0 channel 1/ADC trigger signal 0/SIF/ADC channel 10/ positive input 4 for comparator 0/P0.14
12	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO) /TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel 0 high-side output/UART0 TX(RX)/SPI data output/Timer0 channel 0/ADC trigger signal 1/negative input for comparator 0/P0.15
13	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)	Input/Output	Motor PWM channel 0 low-side output/UART0

No.	Pin Name	Type	Pin Function Description
	/P1.0		TX(RX)/SPI data input/P1.0, with 10k software-enabled built-in pull-up resistor
14	OPA0_IP/P3.5	Input/Output	Positive input for OPA 0/P3.5
15	OPA0_IN/P3.7	Input/Output	Negative input for OPA 0/P3.7
16	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel 11/OPAx output/LDO15 output/P2.7, with 10k software-enabled built-in pull-up resistor
17	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
18	LO3	Output	The low-side gate drive signal output 3 is controlled by the PWM output function of the MCU P1.9 port, that is, GPIO_FBA98[3:0] needs to be configured, and P1.15 shall be set to the output state, i.e. GPIO1_POE [15]. LO3 output will be in the same phase with P1.9 signal, that is, when P1.9 output is '1', and LO3 output is '1'.
19	LO2	Output	The low-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.7 port, that is, GPIO1_F7654[15:12] needs to be configured, and P1.12 shall be set to the output state, i.e. GPIO1_POE[12]. LO2 output will be in the same phase with P1.7 signal, that is, when P1.7 output is '1', and LO2 output is '1'.
20	LO1	Output	The low-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.5 port, that is, GPIO1_F7654[7:4] needs to be configured, and P3.13 shall be set to the output state, i.e. GPIO3_POE[13]. LO1 output will be in the same phase with P1.5 signal, that is, when P1.5 output is '1', and LO1 output is '1'.
21	VS1	Input/Output	High-side floating bias voltage 1
22	HO1	Output	The high-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.4 port, and HO1 output will be in the same phase with P1.4 signal, that is, when input is '1', and HO1 output is '1'.
23	VB1	Input/Output	High-side floating input supply voltage 1
24	VS2	Input/Output	High-side floating bias voltage 2
25	HO2	Output	The high-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.6 port, and HO2 output will be in the same phase with P1.6 signal, that is, when input is '1', and HO2 output is '1'.
26	VB2	Input/Output	High-side floating input supply voltage 2

No.	Pin Name	Type	Pin Function Description
27	VCC	Power	Full-bridge drive module power supply, 4.5 ~ 20V
28	VS3	Input/Output	High-side floating bias voltage 3
29	HO3	Output	The high-side gate drive signal output 3 is controlled by the PWM output function of the MCU P1.8 port, and HO3 output will be in the same phase with P1.8 signal, that is, when input is '1', and HO3 output is '1'.
30	VB3	Input/Output	High-side floating input supply voltage 3
31	OPA2_IP/P3.10	Input/Output	OPA2 positive input/P3.10
32	OPA2_IN/P3.11	Input/Output	OPA2 negative input/P3.11
33	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input/Output	SPI data input/IIC clock/ADC channel 12/positive input 0 for comparator 0/P2.9
34	SPI_DI(DO)/SDA/P2.10	Input/Output	SPI data output/IIC data/P2.10, with 10k software-enabled built-in pull-up resistor
35	OPA3_IN/P3.14	Input/Output	OPA3 negative input/P3.14
36	OPA3_IP/P3.15	Input/Output	OPA3 positive input/P3.15
37	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator 1 output/motor PWM breaking signal 0/SPI chip select signal/voltage reference signal/P2.3
38	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ ADC_TRIG3/CMP1_IP1/P2.4	Input/Output	Hall sensor A-phase input/motor PWM channel 2 high-side output/UART1 TX(RX)/Timer1 channel 0/ADC trigger signal 3/positive input 1 for comparator 1/P2.4, with a 10k software-enabled built-in pull-up resistor
39	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/P2.5/TIM3_CH0/P2.6/TIM3_CH1/P2.13	Input/Output	Hall sensor B-phase input/motor PWM channel 2 low side/UART1 TX(RX)/Timer1 channel 1/ADC trigger signal 0/positive input 2 for comparator 1/P2.5/Timer3 Channel 0/P2.6/Timer3 Channel 1/P2.13, with a 10k software-enabled built-in pull-up resistor
40	SWCLK	Input	SWD clock, with 10k built-in pull-up resistor

3.1.3 LKS32MC086N8Q8(B)

Fig. 3-2 LKS32MC086N8Q8(B) Pin Assignment

Table 3-2 LKS32MC086N8Q8(B) Pin Function Description

No.	Item	Type	Function
0	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
1	ADC_CH4/DAC_OUT/P0.0	Input/Output	ADC channel 4/DAC output/P0.0, with a 10k software-enabled built-in pull-up resistor
2	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor.
3	AVDD	Power	Chip power input, voltage range 2.2 ~ 5.5V(B-version

No.	Item	Type	Function
			chip is powered by 3.0V~5.5V). Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
4	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	IIC clock/Timer2 channel 0/ADC channel 7/P0.3
5	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	IIC data/Timer2 channel 1/ADC channel 8/P0.4
6	ADC_CH9/P0.5	Input/Output	ADC channel 9/P0.5
7	UART1_TX(RX)/TIM1_CH0/CAN_RX/P0.6	Input/Output	UART1 TX(RX)/Timer1 channel 0/CAN_RECEIVE/P0.6, with a 10k software-enabled built-in pull-up resistor
8	UART1_TX(RX)/TIM1_CH1/CAN_TX/P0.7	Input/Output	UART1 TX(RX)/Timer1 channel 1/CAN_SEND/P0.7, with a 10k software-enabled built-in pull-up resistor
9	MCPWM_CH1P/TIM2_CH0/P2.11	Input/Output	Motor PWM channel 1 high-side output/Timer 2 channel 0/P2.11
10	MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	Input/Output	Motor PWM channel 1 low-side output/Timer2 channel 1/ADC trigger signal 2/P2.12
11	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P 0.11	Input/Output	Hall sensor A-phase input/Timer3 channel 0/ADC channel 15/positive input 1 for comparator 0/P0.11
12	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/C AN_RX/P0.12	Input/Output	Hall sensor B-phase input/Timer3 channel 1/ADC channel 16/positive input 2 for comparator 0/CAN_RECEIVE/P0.12
13	HALL_IN2/ADC_CH17/CMP0_IP3/CAN_TX/P0.1 3	Input/Output	Hall sensor C-phase input/ADC channel 17/positive input 3 for comparator 0/CAN_SEND/P0.13
14	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH 1/ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.1 4	Input/Output	Comparator 0 output/motor PWM breaking signal 1/SPI clock/Timer0 channel 1/ADC trigger signal 0/ISDN/ADC channel 10/positive input 4 for comparator 0/P0.14
15	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TI M0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel 0 high-side output/UART0 (TX)RX/SPI data input(output)/Timer0 channel 0/ADC trigger signal 1/negative input for comparator 0/P0.15
16	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1 .0	Input/Output	Motor PWM channel 0 low-side output/UART 0 TX(RX)/SPI data input(output)/P1.0, with a 10k software-enabled built-in pull-up resistor
17	OPA0_IP/P3.5	Input/Output	OPA0 positive input/P3.5
18	OPA0_IN/P3.7	Input/Output	OPA0 negative input/P3.7
19	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel 11/OPAx output/LDO15 output/P2.7, with a 10k software-enabled built-in pull-up resistor
20	OPA1_IP/P3.0/UART1_TX(RX)/TIM3_CH1/OSC_ OUT/P3.9	Input/Output	OPA1 positive input/P3.0/ UART1 TXD/Timer3 channel1/Crystal Oscillator Output/P3.9, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
21	OPA1_IN/P3.1/UART1_TX(RX)/TIM3_CH0/OSC_ IN/P2.8	Input/Output	OPA 1 negative input/P3.1/ UART1 RXD/Timer3 channel0/Crystal Oscillator Input/P2.8, with a 10k software-controllable built-in pull-up resistor, if

No.	Item	Type	Function
			connected to a crystal, add a 15pf shut capacitor to ground
22	VCC	Power	Full-bridge drive module power supply, 10 ~ 20V
23	LO1	Output	The low-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.5 port, that is, GPIO1_F7654[7:4] needs to be configured, and P3.13 shall be set to the output state, i.e. GPIO3_POE[13]. LO1 output will have different polaity with P1.5 signal, that is, when input '0', and LO1 output is '1'.
24	LO2	Output	The low-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.7 port, that is, GPIO1_F7654[15:12] needs to be configured, and P1.12 shall be set to the output state, i.e. GPIO1_POE[12]. LO2 output will have different polaity with P1.7 signal, that is, when input '0', and LO2 output is '1'.
25	LO3	Output	The low-side gate drive signal output 3 is controlled by the PWM output function of the MCU P1.9 port, that is, GPIO_FBA98 [3:0] needs to be configured, and P1.15 shall be set to the output state, i.e. GPIO1_POE [15]. LO3 output will have different polaity with P1.9 signal, that is, when input '0', and LO3 output is '1'.
26	VS1	Input/Output	High-side floating bias voltage 1
27	HO1	Output	The high-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.4 port, and HO1 output will have different polaity with P1.4 signal, that is, when input is '1', and HO1 output is '1'.
28	VB1	Input/Output	High-side floating input supply voltage 1
29	VS2	Input/Output	High-side floating bias voltage 2
30	HO2	Output	The high-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.6 port, and HO2 output will have different polaity with P1.6 signal, that is, when input is '1', and HO2 output is '1'.
31	VB2	Input/Output	High-side floating input supply voltage 2
32	VS3	Input/Output	High-side floating bias voltage 3
33	HO3	Output	The high-side gate drive signal output 3 is controlled by the PWM output function of the MCU P1.8 port, and HO3 output will have different polaity with P1.8 signal, that is, when input is '1', and HO3 output is '1'.
34	VB3	Input/Output	High-side floating input supply voltage 3
35	NC	NC	No connection
36	MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0 /ADC_TRIG2/P1.10	Input/Output	Motor PWM channel 3 high-side output/UART 0 (TX)RX/IIC clock/Timer0 channel 0/ADC trigger signal 2/P1.10, with a 10k software-enabled built-in pull-up

No.	Item	Type	Function
			resistor
37	MCPWM_CH3N/UART0_TX(RX)/SDA/TIM0_CH 1/ADC_TRIG3/SIF/P1.11	Input/Output	Motor PWM channel 3 low-side output/UART 0 TX(RX)/IIC data/Timer0 channel 1/ADC trigger signal 3/P1.11, with a 10k software-enabled built-in pull-up resistor
38	OPA2_IP/P3.10	Input/Output	OPA2 positive input/P3.10
39	OPA2_IN/P3.11	Input/Output	OPA2 negative input/P3.11
40	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input/Output	SPI data input(output)/IIC clock/ADC channel 12/positive input 0 for comparator 0/P2.9
41	SPI_DI(DO)/SDA/P2.10	Input/Output	SPI data output/IIC data/P2.10, with a 10k software-enabled built-in pull-up resistor
42	OPA3_IN/P3.14	Input/Output	OPA3 negative input/P3.14
43	OPA3_IP/P3.15	Input/Output	OPA3 positive input/P3.15
44	SPI_CLK/ADC_CH14/CMP1_IP0/P2.1	Input/Output	SPI clock/ADC channel 14/positive input for comparator 1/P2.1, with a 10k software-enabled built-in pull-up resistor
45	CMP1_IN/P2.2	Input/Output	Comparator 1 negative input/P2.2
46	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator 1 output/motor PWM termination signal 0/SPI chip select signal/voltage reference signal/P2.3
47	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM 1_CH0/ ADC_TRIG3/CMP1_IP1/CAN_RX/P2.4	Input/Output	Hall sensor A-phase input/motor PWM channel 2 high-side output/UART 1 (TX)RX/Timer1 channel 0/ADC trigger signal 3/positive input 1 for comparator 1/CAN_RECEIVE/P2.4, with a 10k software-enabled built-in pull-up resistor
48	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM 1_CH1/ADC_TRIG0/CMP1_IP2/CAN_TX/P2.5	Input/Output	Hall sensor B-phase input/motor PWM channel 2 low-side output/UART 1 TX(RX)/Timer1 channel 1/ADC trigger signal 0/positive input 2 for comparator 1/CAN_SEND/P2.5, with a 10k software-enabled built-in pull-up resistor
49	HALL_IN2/MCPWM_CH3P/TIM3_CH0/ ADC_TRIG1/CMP1_IP3/P2.6	Input/Output	Hall sensor C-phase input/motor PWM channel 3 high-side output/Timer3 channel 0/ADC trigger signal 1/positive input 3 for comparator 1/P2.6, with a 10k software-enabled built-in pull-up resistor
50	SWCLK	Input	SWD clock with 10k built-in pull-up resistor
51	SWDIO/SCL/P2.14	Input/Output	SWD data/IIC clock/P2.14 with 10k built-in pull-up resistor
52	SDA/P2.15	Input/Output	IIC data/P2.15

3.1.4 LKS32MC088KU8Q8(B)

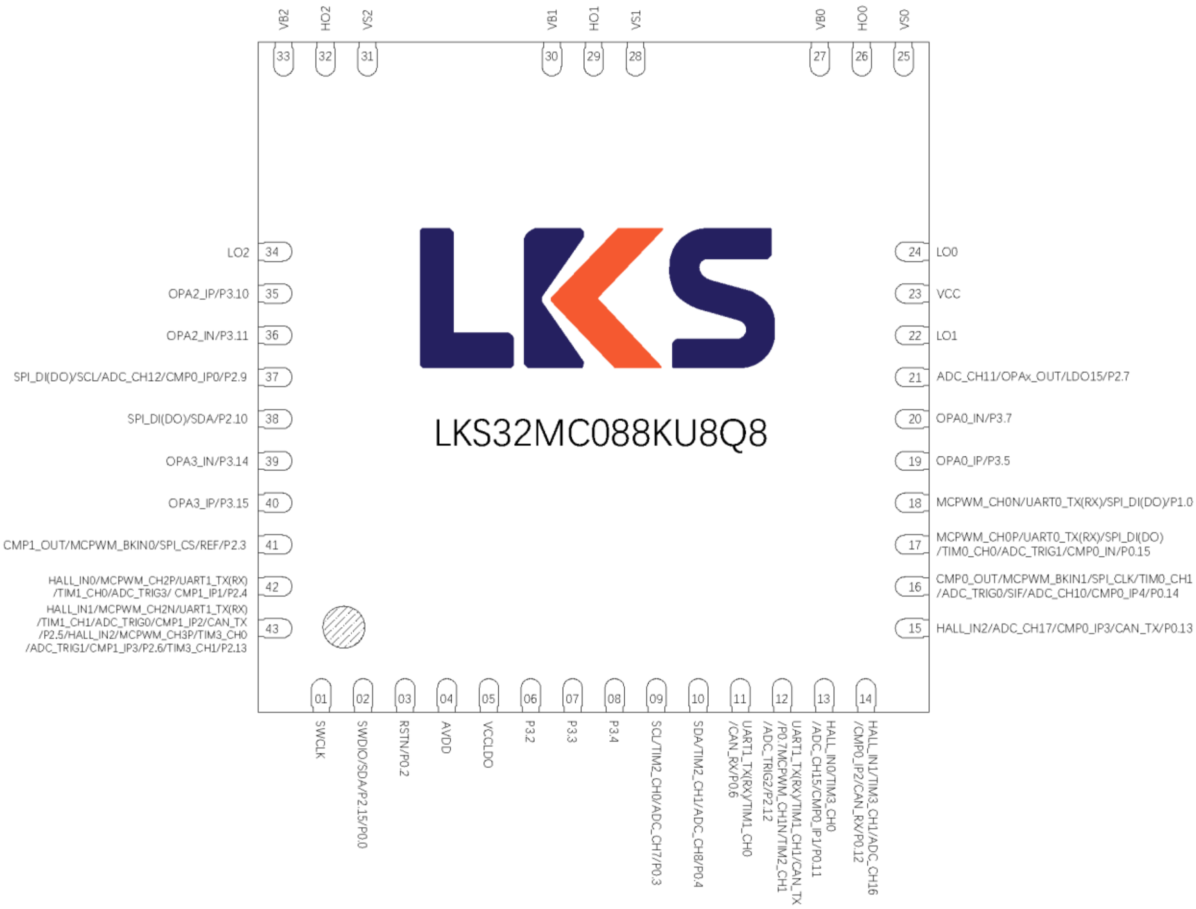

Fig. 3-3 LKS32MC088KU8Q8(B) Pin Assignment

Table 3-3 LKS32MC086N8Q8(B) Pin Function Description

No.	Item	Type	Function
0	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
1	SWCLK	Input	SWD clock with built-in 10K resistor fixed pull-up
2	SWDIO/SDA/P2.15/P0.0	Input /Output	SWD data /IIC data /P2.15/ P0.0, built-in 10K resistor with fixed pull-up.
3	RSTN/P0.2	Input /Output	RSTN/P0.2, which is used as RSTN by default, can be externally connected with a capacitor of 10nF~100nF to the ground, and an internal pull-up resistor of 100K. It is recommended to put a pull-up resistor of 10K ~ 20K between RSTN and AVDD on PCB. If there is a pull-up resistor outside, the capacitor of RSTN is fixed to 100nF.
4	AVDD	Power	LDO 5V power output, off-chip decoupling capacitance ⩾1uF, and as close as possible to the AVDD pin.
5	VCCLDO	Input Power	5V LDO input power supply, the input power range is 7-20 v, the maximum output current capacity is 80mA. The off-chip

No.	Item	Type	Function
			decoupling capacitance is recommended to be >0.33uF and as close as possible to the VCCLDO pin.
6	P3.2	Input /Output	P3.2
7	P3.3	Input /Output	P3.3
8	P3.4	Input /Output	P3.4
9	SCL/TIM2_CH0/ADC_CH7/P0.3	Input /Output	IIC clock /Timer2 channel 0/ADC channel 7/P0.3
10	SDA/TIM2_CH1/ADC_CH8/P0.4	Input /Output	IIC data /Timer2 channel 1/ADC channel 8/P0.4
11	UART1_TX(RX)/TIM1_CH0/CAN_RX/P0.6	Input /Output	UART1_TX(RX)/Timer1 channel 0/CAN receive /P0.6, built-in 10K pull-up resistor that CAN be opened by software
12	UART1_TX(RX)/TIM1_CH1/CAN_TX/P0.7/MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	Input /Output	UART1_TX(RX)/Timer1 channel 1/CAN send /P0.7, built-in 10K pull-up resistor that CAN be opened by software Motor PWM channel 1 low side /Timer2 channel 1/ADC trigger signal 2/P2.12
13	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input /Output	Hall sensor phase A input /Timer3 channel 0/ADC channel 15/ Comparator 0 in-phase input channel 1/P0.11
14	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/CAN_RX/P0.12	Input /Output	Hall sensor B phase input /Timer3 channel 1/ ADC channel 16/ Comparator 0 in-phase input channel 2/CAN receive /P0.12
15	HALL_IN2/ADC_CH17/CMP0_IP3/CAN_TX/P0.13	Input /Output	Hall sensor C phase input/ADC channel 17/ Comparator 0 in-phase input channel 3/CAN transmit /P0.13
16	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input /Output	Comparator 0 output/motor PWM termination signal 1/SPI clock /Timer0 channel 1/ADC trigger signal 0/ one-line pass /ADC channel 10/ Comparator 0 in-phase input channel 4/P0.14
17	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input /Output	Motor PWM channel 0 high edge /UART0_TX(RX)/ SPI_DI(DO)/ Timer0 channel 0/ADC trigger signal 1/ comparator 0 negative input /P0.15
18	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	Input /Output	Motor PWM channel 0 low side /UART0_TX(RX)/ SPI_DI(DO)/ P1.0, built-in software open 10K pull-up resistance
19	OPA0_IP/P3.5	Input /Output	Opamp 0 in-phase input /P3.5
20	OPA0_IN/P3.7	Input /Output	Opamp 0 inverse-phase input /P3.7
21	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input /Output	ADC channel 11/OPAx output /LDO15 output /P2.7, built-in 10K pull-up resistor that can be turned on by software
22	LO1	Output	The low-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.7 port, that is, GPIO1_F7654[15:12] needs to be configured, and P1.12 shall be set to the output state, i.e. GPIO1_POE[12]. LO2 output will be in the same phase with P1.7 signal, that is, when P1.7 output is '1', and LO2 output is '1'.
23	VCC	Power	Full bridge drive module power supply, 10~20V
24	LO0	Output	The low-side gate drive signal output 0 is controlled by the PWM output function of the MCU P1.5 port, that is, GPIO1_F7654[7:4] needs to be configured, and P3.13 shall be set to the output state, i.e. GPIO3_POE[13]. LO1 output will be

No.	Item	Type	Function
			in the same phase with P1.5 signal, that is, when P1.5 output is '1', and LO1 output is '1'.
25	VS0	Input /Output	High side floating bias voltage 0
26	HO0	Output	High side gate drive signal output 0, controlled by MCU P1.4 port output signal, HO0 output and P1.4 signal is in the same phase relationship, that is, when the input is' 1 ', HO0 output '1'.
27	VB0	Input /Output	The high-side floating input voltage is 0
28	VS1	Input /Output	High side floating bias voltage 1
29	HO1	Output	High-side gate drive signal output 1, controlled by MCU P1.6 port output signal, HO1 output and P1.6 signal are in the same phase relationship, that is, when the input is' 1 ', HO1 output '1'.
30	VB1	Input /Output	The floating input voltage on the high side is 1
31	VS2	Input /Output	High side floating bias voltage 2
32	HO2	Output	High-side gate drive signal output 2, controlled by MCU P1.8 port output signal, HO2 output and P1.8 signal is in the same phase relationship, that is, when the input is' 1 ', HO2 output '1'.
33	VB2	Input /Output	The floating input voltage on the high side is 2
34	LO2	Output	The low-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.9 port, that is, GPIO_FBA98[3:0] needs to be configured, and P1.15 shall be set to the output state, i.e. GPIO1_POE [15]. LO3 output will be in the same phase with P1.9 signal, that is, when P1.9 output is '1', and LO3 output is '1'.
35	OPA2_IP/P3.10	Input /Output	Opamp 2 in-phase input /P3.10
36	OPA2_IN/P3.11	Input /Output	Opamp 2 inverting end input /P3.11
37	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input /Output	SPI_DI(DO)/IIC clock /ADC channel 12/ Comparator 0 in-phase input channel 0/P2.9
38	SPI_DI(DO)/SDA/P2.10	Input /Output	SPI_DI(DO)/IIC data /P2.10, built-in 10K pull-up resistor that can be turned on by software
39	OPA3_IN/P3.14	Input /Output	Opamp 3 inverting end input /P3.14
40	OPA3_IP/P3.15	Input /Output	Opamp 3 in-phase input /P3.15
41	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input /Output	Comparator 1 output/motor PWM stop signal 0/SPI chip selector/voltage reference signal /P2.3
42	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/ CMP1_IP1/CAN_RX/P2.4	Input /Output	Hall sensor A-phase input/motor PWM channel 2 high-edge /UART1_TX(RX)/Timer1 channel 0/ADC trigger signal 3/ Comparator 1 in-phase input channel 1/CAN receive /P2.4, built-in 10K pull-up resistor that CAN be opened by software
43	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/CAN_TX/P2.5/HALL_IN2/MCPWM_CH3P/TIM3_CH0/ADC_TRIG1/CMP1_IP3/P2.6/TIM3_CH1/P2.13	Input /Output	Hall sensor B phase input/motor PWM channel 2 low side /UART1_TX(RX)/Timer1 channel 1/ADC trigger signal 0/ Comparator 1 in-phase input channel 2/CAN send /P2.5, built-in 10K pull-up resistor that CAN be opened by software Hall sensor C phase input/motor PWM channel 3 high side /Timer3 channel 0/ADC trigger signal 1/ Comparator 1

No.	Item	Type	Function
			in-phase input channel 3/P2.6, built-in 10K pull-up resistor that can be opened by software Timer3 channel 1/ P2.13

3.1.5 LKS32MC088K22U8Q8

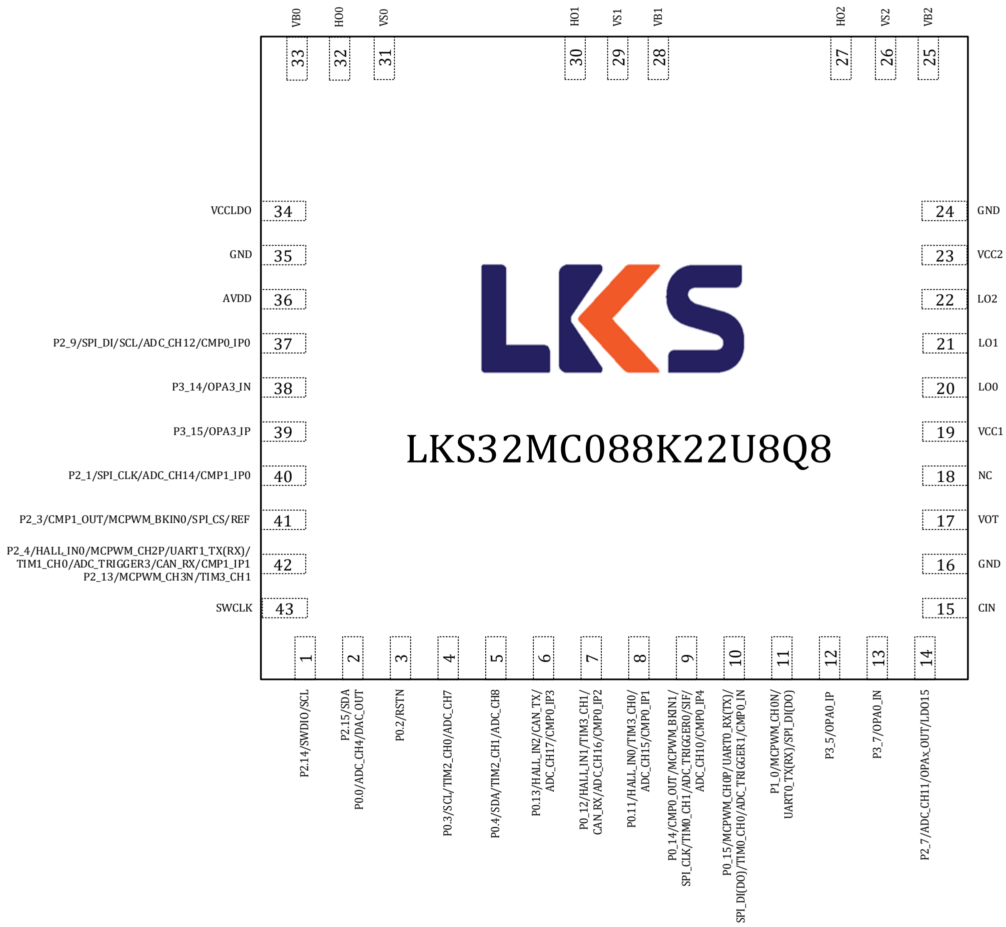

Fig. 3-3 LKS32MC088K22U8Q8 Pin Assignment

Table 3-3 LKS32MC088K22U8Q8 Pin Function Description

No.	Item	Type	Function
0	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
1	P2.14/SWDIO/SCL	Input /Output	SWD clock with built-in 10K resistor fixed pull-up
2	P2.15/SDA P0.0/ADC_CH4/DAC_OUT	Input /Output	IIC data /P2.15/ P0.0, built-in 10K resistor with fixed pull-up, ADC channel 4/DAC output/P0.0.
3	P0.2/RSTN	Input /Output	RSTN/P0.2, which is used as RSTN by default, can be externally connected with a capacitor of 10nF~100nF to the ground, and an internal pull-up resistor of 100K. It is recommended to put a pull-up resistor of 10K ~ 20K between RSTN and AVDD on PCB.

No.	Item	Type	Function
			If there is a pull-up resistor outside, the capacitor of RSTN is fixed to 100nF.
4	P0.3/SCL/TIM2_CH0/ADC_CH7	Input /Output	IIC clock /Timer2 channel 0/ADC channel 7/P0.3
5	P0.4/SDA/TIM2_CH1/ADC_CH8	Input /Output	IIC data /Timer2 channel 1/ADC channel 8/P0.4
6	P0.13/HALL_IN2/CAN_TX/ADC_CH17/CMP0_IP3	Input /Output	Hall sensor C phase input/ADC channel 17/ Comparator 0 in-phase input channel 3/CAN transmit /P0.13
7	P0_12/HALL_IN1/TIM3_CH1/CAN_RX/ADC_CH16/ CMP0_IP2	Input /Output	Hall sensor B phase input /Timer3 channel 1/ ADC channel 16/ Comparator 0 in-phase input channel 2/CAN receive /P0.12
8	P0.11/HALL_IN0/TIM3_CH0/ADC_CH15 /CMP0_IP1	Input /Output	Hall sensor phase A input /Timer3 channel 0/ADC channel 15/ Comparator 0 in-phase input channel 1/P0.11
9	P0_14/CMP0_OUT/MCPWM_BKIN1/SPI_CLK/ TIM0_CH1/ADC_TRIGGER0/SIF/ ADC_CH10/CMP0_IP4	Input /Output	Comparator 0 output/motor PWM termination signal 1/SPI clock /Timer0 channel 1/ADC trigger signal 0/ one-line pass /ADC channel 10/ Comparator 0 in-phase input channel 4/P0.14
10	P0_15/MCPWM_CH0P/UART0_RX(TX)/SPI_DI(DO)/ TIM0_CH0/ADC_TRIGGER1/CMP0_IN	Input /Output	Motor PWM channel 0 high edge /UART0_TX(RX)/ SPI_DI(DO)/ Timer0 channel 0/ADC trigger signal 1/ comparator 0 negative input /P0.15
11	P1_0/MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)	Input /Output	Motor PWM channel 0 low side /UART0_TX(RX)/ SPI_DI(DO)/ P1.0, built-in software open 10K pull-up resistance
12	P3_5/OPA0_IP	Input /Output	Opamp 0 in-phase input /P3.5
13	P3_7/OPA0_IN	Input /Output	Opamp 0 inverse-phase input /P3.7
14	P2_7/ADC_CH11/OPAx_OUT/LDO15	Input /Output	ADC channel 11/OPAx output /LDO15 output /P2.7, built-in 10K pull-up resistor that can be turned on by software
15	CIN	Input	Current sense input
16	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
17	VOT	Output	Temperature sensing output
18			
19	VCC	Power	Full bridge drive module power supply, 10~20V
20	LO0	Output	The low-side gate drive signal output 0 is controlled by the PWM output function of the MCU P1.5 port, that is, GPIO1_F7654[7:4] needs to be configured, and P3.13 shall be set to the output state, i.e. GPIO3_POE[13]. LO1 output will be in the same phase with P1.5 signal, that is, when P1.5 output is '1', and LO1 output is '1'.
21	LO1	Output	The low-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.7 port, that is, GPIO1_F7654[15:12] needs to be configured, and P1.12 shall be set to the output state, i.e. GPIO1_POE[12]. LO2 output will be in the same phase with P1.7 signal, that is, when P1.7 output is

No.	Item	Type	Function
			'1', and LO2 output is '1'.
22	LO2	Output	The low-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.9 port, that is, GPIO_FBA98[3:0] needs to be configured, and P1.15 shall be set to the output state, i.e. GPIO1_POE [15]. LO3 output will be in the same phase with P1.9 signal, that is, when P1.9 output is '1', and LO3 output is '1'.
23	VCC	Power	Full bridge drive module power supply, 10~20V
24	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
25	VB2	Input /Output	The floating input voltage on the high side is 2
26	VS2	Input /Output	High side floating bias voltage 2
27	HO2	Output	High-side gate drive signal output 2, controlled by MCU P1.8 port output signal, HO2 output and P1.8 signal is in the same phase relationship, that is, when the input is' 1 ', HO2 output '1'.
28	VB1	Input /Output	The floating input voltage on the high side is 1
29	VS1	Input /Output	High side floating bias voltage 1
30	HO1	Output	High-side gate drive signal output 1, controlled by MCU P1.6 port output signal, HO1 output and P1.6 signal are in the same phase relationship, that is, when the input is' 1 ', HO1 output '1'.
31	VS0	Input /Output	High side floating bias voltage 0
32	HO0	Output	High side gate drive signal output 0, controlled by MCU P1.4 port output signal, HO0 output and P1.4 signal is in the same phase relationship, that is, when the input is' 1 ', HO0 output '1'.
33	VB0	Input /Output	The floating input voltage on the high side is 0
34	VCCLDO	Input Power	5V LDO input power supply, the input power range is 7-20 v, the maximum output current capacity is 80mA. The off-chip decoupling capacitance is recommended to be >0.33uF and as close as possible to the VCCLDO pin.
35	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
36	AVDD	Power	LDO 5V power output, off-chip decoupling capacitance ⩾1uF, and as close as possible to the AVDD pin.
37	P2_9/SPI_DI/SCL/ADC_CH12/CMP0_IP0	Input /Output	SPI_DI(DO)/IIC clock /ADC channel 12/ Comparator 0 in-phase input channel 0/P2.9
38	P3_14/OPA3_IN	Input /Output	Opamp 3 inverting end input /P3.14
39	P3_15/OPA3_IP	Input /Output	Opamp 3 in-phase input /P3.15
40	P2_1/SPI_CLK/ADC_CH14/CMP1_IP0	Input /Output	SPI clock/ADC channel 14/positive input for comparator 1/P2.1, with a 10k software-enabled built-in pull-up resistor
41	P2_3/CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF	Input /Output	Comparator 1 output/motor PWM stop signal 0/SPI chip selector/voltage reference signal /P2.3
42	P2_4/HALL_IN0/MCPWM_CH2P/	Input /Output	Hall sensor A-phase input/motor PWM channel 2 high-edge

No.	Item	Type	Function
	UART1_TX(RX)/ TIM1_CH0/ADC_TRIGGER3/CAN _RX/CMP1_IP1 P2_13/MCPWM_CH3N/TIM3_CH 1		/UART1_TX(RX)/Timer1 channel 0/ADC trigger signal 3/ Comparator 1 in-phase input channel 1/CAN receive /P2.4, built-in 10K pull-up resistor that CAN be opened by software Motor PWM channel 0 low side/Timer3 channel 1/ P2.13
43	SWCLK	Input	SWD clock with built-in 10K resistor fixed pull-up

3.2 Description of Pin Multiplex Function

LKS32MC086(A)N8Q8(B) and LKS32MC084F6Q8(B) share the same pin multiplex function.

Table 3-3 LKS32MC086N8Q8(B) Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P0.0												ADC_CH4, DAC_OUT
P0.1												ADC_CH6
P0.2												
P0.3						SCL		TIM2_CH0				ADC_CH7
P0.4						SDA		TIM2_CH1				ADC_CH8
P0.5												ADC_CH9
P0.6				UART1_TX(RX)			TIM1_CH0			CAN_RX		
P0.7				UART1_TX(RX)			TIM1_CH1			CAN_TX		
P0.8												
P0.9						SCL		TIM2_CH0				
P0.10						SDA		TIM2_CH1				
P0.11		HALL_IN0						TIM3_CH0				ADC_CH15/CMP0_IP1
P0.12		HALL_IN1						TIM3_CH1		CAN_RX		ADC_CH16/CMP0_IP2
P0.13		HALL_IN2								CAN_TX		ADC_CH17/CMP0_IP3
P0.14	CMP0_OUT		MCPWM_BKIN1		SPI_CLK		TIM0_CH1		ADC_TRIG0		SIF	ADC_CH10/CMP0_IP4
P0.15			MCPWM_CH0P	UART0_TX(RX)	SPI_DI(DO)		TIM0_CH0		ADC_TRIG1			CMP0_IN

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P1.0			MCPWM_CH0N	UART0_TX(RX)	SPI_DI(DO)							
P1.1					SPI_CS							
P1.2								TIM3_CH0				
P1.3								TIM3_CH1				ADC_CH5
P1.4	LRC		MCPWM_CH0P									
P1.5	HRC		MCPWM_CH0N									
P1.6			MCPWM_CH1P									
P1.7			MCPWM_CH1N									
P1.8			MCPWM_CH2P									
P1.9			MCPWM_CH2N									
P1.10			MCPWM_CH3P	UART0_TX(RX)		SCL	TIM0_CH0		ADC_TRIG2			ADC_CH13
P1.11			MCPWM_CH3N	UART0_TX(RX)		SDA	TIM0_CH1		ADC_TRIG3		SIF	
P1.12			MCPWM_CH1N									
P1.13					SPI_CLK		TIM0_CH0					
P1.14					SPI_DI(DO)		TIM0_CH1					
P1.15			MCPWM_CH2N									

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P2.0					SPI_CS			TIM2_CH1				
P2.1					SPI_CLK							ADC_CH14/ CMP1_IP0
P2.2												CMP1_IN
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS							REF
P2.4		HALL_IN0	MCPWM_CH2P	UART1_TX(RX)			TIM1_CH0		ADC_TRIG3	CAN_RX		CMP1_IP1
P2.5		HALL_IN1	MCPWM_CH2N	UART1_TX(RX)			TIM1_CH1		ADC_TRIG0	CAN_TX		CMP1_IP2
P2.6		HALL_IN2	MCPWM_CH3P					TIM3_CH0	ADC_TRIG1		SIF	CMP1_IP3
P2.7												ADC_CH11/ OPAx_OUT/ LDO15
P2.8				UART1_TX(RX)				TIM3_CH0				OSC_IN
P2.9					SPI_DI(DO)	SCL						ADC_CH12/ CMP0_IP0
P2.10					SPI_DI(DO)	SDA						
P2.11			MCPWM_CH1P					TIM2_CH0				
P2.12			MCPWM_CH1N					TIM2_CH1	ADC_TRIG2			
P2.13			MCPWM_CH3N					TIM3_CH1				
P2.14						SCL						
P2.15						SDA						

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P3.0												OPA1_IP
P3.1												OPA1_IN
P3.2												
P3.3												
P3.4												
P3.5												OPA0_IP
P3.6												
P3.7												OPA0_IN
P3.8												
P3.9				UART1_TX(RX)				TIM3_CH1				OSC_OUT
P3.10												OPA2_IP
P3.11												OPA2_IN
P3.12												
P3.13	HRC		MCPWM_CH0N									
P3.14												OPA3_IN
P3.15												OPA3_IP

4 Package Size

4.1 LKS32MC084DF6Q8(B)

QFN5*5 40L-0.75 Profile Quad Flat Package:

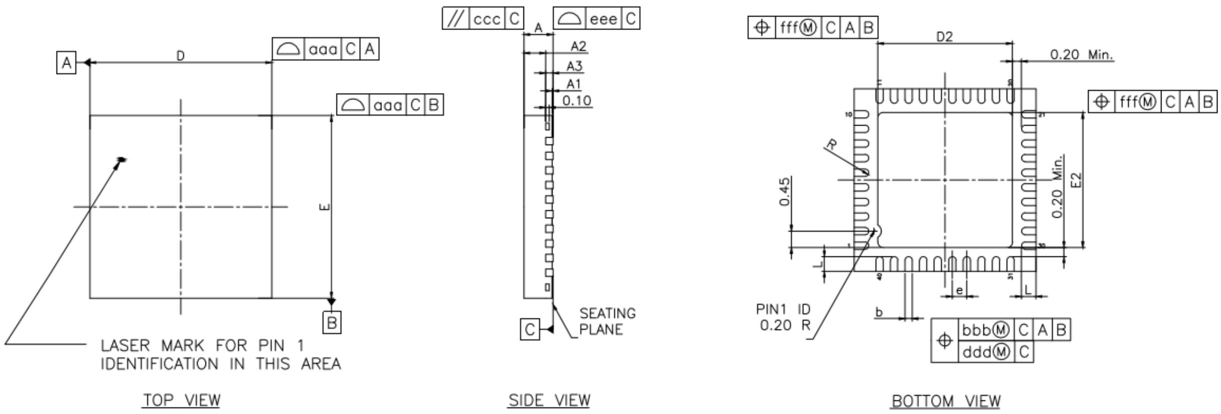

Fig. 4-1 LKS32MC084DF6Q8(B) Package Diagram

Table 4-1 LKS32MC084DF6Q8(B) Package Dimension

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.95	0.028	0.030	0.037
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	0.50	0.55	0.75	0.020	0.022	0.030
A3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	3.20	3.70	3.80	0.126	0.146	0.150
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.20	3.70	3.80	0.126	0.146	0.150
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.4 bsc			0.016 bsc		
R	0.075	-	-	0.003	-	-
TOLERANCE OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

4.2 LKS32MC086N8Q8(B)

QFN6*6 52L-0.55 Profile Quad Flat Package:

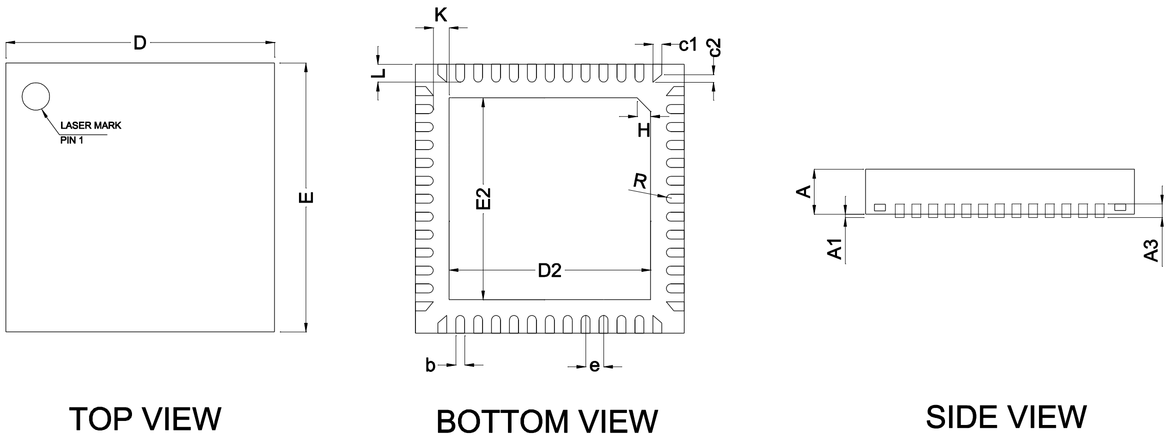

Fig. 4-2 LKS32MC086N8Q8(B) Package Diagram

Table 4-2 LKS32MC086N8Q8(B) Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
e	0.30	0.40	0.45
H	0.35REF		
K	0.25	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.17	-
c2	-	0.17	-

4.3 LKS32MC088KU8Q8(B)

QFN43L Profile Quad Flat Package:

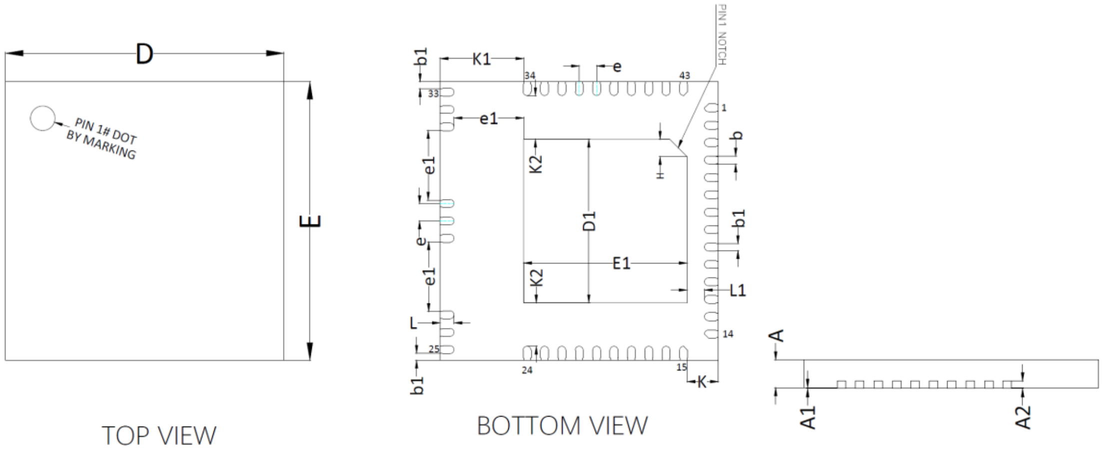

Fig. 4-3 LKS32MC088KU8Q8(B) Package Diagram

Table 4-3 LKS32MC088KU8Q8(B) Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2	0.203REF		
b	0.18	0.23	0.28
b1	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	0.50BSC		
e1	2.00BSC		
D1	4.60	4.70	4.80
E1	4.60	4.70	4.80
L	0.30	0.40	0.50
L1	0.45	0.50	0.55
K	0.90BSC		
K1	2.40BSC		
K2	1.25BSC		
H	0.50BSC		

4.4 LKS32MC088K22U8Q8

QFN43L Profile Quad Flat Package:

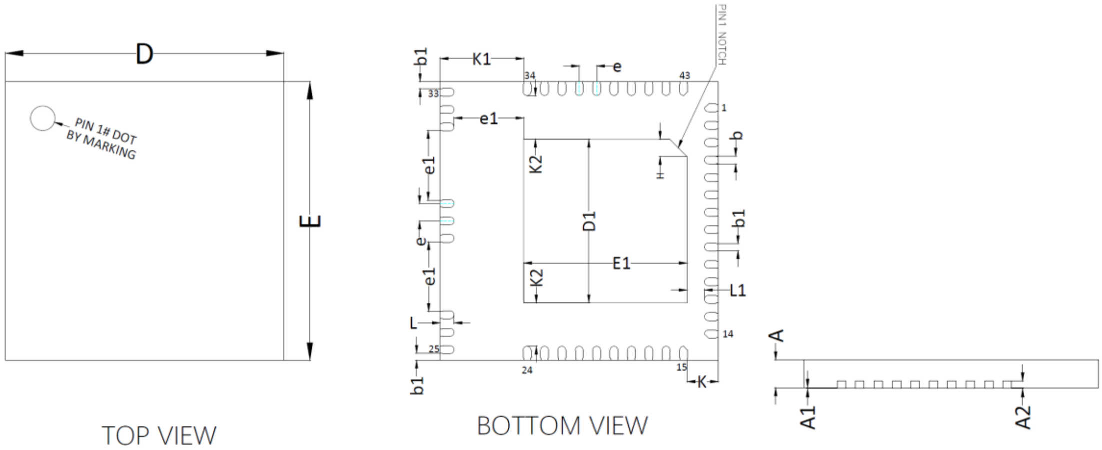

图 4-3 LKS32MC088K22U8Q8 封装图示

表 4-3 LKS32MC088K22U8Q8 封装尺寸

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2	0.203REF		
b	0.18	0.23	0.28
b1	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	0.50BSC		
e1	2.00BSC		
D1	4.60	4.70	4.80
E1	4.60	4.70	4.80
L	0.30	0.40	0.50
L1	0.45	0.50	0.55
K	0.90BSC		
K1	2.40BSC		
K2	1.25BSC		
H	0.50BSC		

5 Electrical Characteristics

The electrical characteristics of integrated 6N Driver for LKS32MC086/084D are shown in the following table. Take the LKS32MC086N8Q8(B) for an example.

Table 5-1 LKS32MC086N8Q8(B) electrical absolute characteristics

Parameter	Min.	Max.	Unit	Description
MCU Power Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Power Supply Voltage (VCC)	-0.3	+25.0	V	
Operating Temperature	-40	+105	˚C	
Storage Temperature	-40	+150	˚C	
Junction Temperature	-	150	°C	
Pin Temperature (solder for10 seconds)	-	260	°C	

Table 5-2 LKS32MC086N8Q8(B) Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Power supply voltage (AVDD)	3.0	5	5.5	V	The AVDD reset level of version A chip is 2.2V ± 0.2V
	2.2				The AVDD reset level of version B chip is 2.7V ± 0.2V
Analog Power Supply Voltage ($AVDD_A$)	3.3	5	5.5	V	ADC use 2.4V internal reference
	2.8	5	5.5	V	ADC use 1.2V internal reference
Gate Driver Power supply voltage (VCC)	4.5		20	V	

OPA could work under 2.2V, but the output range will be limited.

Table 5-3 LKS32MC086N8Q8(B) Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Power Supply Voltage (AVDD)	2.2	5	5.5	V	
Analog Supply Voltage ($AVDD_A$)	2.8	5	5.5	V	

OPA could work under 2.2V, but the output range will be limited.

Table 5-4 LKS32MC086N8Q8(B) ESD parameters

Item	Min.	Max.	Unit
ESD test (HBM)	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-5 LKS32MC086N8Q8(B) IO absolute characteristics

Parameter	Description	Min.	Max.	Unit

$V_{IN\text{-}GPIO}$	GPIO Signal Input Voltage Range	-0.3	6.0	V
I_{INJ_PAD}	Maximum Injection Current of A Single GPIO	-11.2	11.2	mA
I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 5-6 LKS32MC086N8Q8(B) IO DC Parameters

Parameter	Description	AVDD	Conditions	Min.		Max.	Unit
V_{IH}	High input level of digital IO	5V	-	0.7*AVDD			V
V_{IH}	High input level of digital IO	3.3V	-	2.0			V
V_{IL}	Low input level of digital IO	5V	-			0.3*AVDD	V
V_{IL}	Low input level of digital IO	3.3V	-			0.8	V
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD			V
V_{HYS}	Schmidt hysteresis range	3.3V	-	0.1*AVDD			V
I_{IH}	Digital IO current consumption when input is high	5V	-			1	uA
I_{IH}	Digital IO current consumption when input is high	3.3V	-			1	uA
I_{IL}	Digital IO current consumption when input is low	5V	-	-1			uA
I_{IL}	Digital IO current consumption when input is low	3.3V	-	-1			uA
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8			V
V_{OL}	Low output level of digital IO		Current = 11.2mA			0.5	V
R_{pup}	Pull-up resistor* — Reset pin			100	200	400	kΩ
R_{pup}	Pull-up resistor* — Normal pin			8	10	12	kΩ
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit			100		200	Ω
C_{IN}	Digital IO Input-capacitance	5V	-			10	pF
C_{IN}	Digital IO Input-capacitance	3.3V	-			10	pF

* Only some IOs have built-in pull-up resistors, see section “Pin Function Description” for details.

6 Analog Characteristics

The analog characteristics of integrated 6N Driver for LKS32MC086/084D are shown in the following table. Take the LKS32MC086N8Q8(B) as an example.

Table 6-1 LKS32MC086N8Q8(B) analog characteristics

Parameter	Min.	Normal	Max.	Unit	Description
Analog-to-Digital Converter (ADC)					
Power Supply	2.8	5	5.5	V	ADC use 2.4V internal reference
	3.3	5	5.5	V	ADC use 1.2V internal reference
Sampling rate		3		MHz	f_{adc}/16
Differential input signal range	-2.352		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-3.528		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
Single-ended input signal range	-0.3		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-0.3		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
	-0.3		AVDD*0.9	V	REF2VDD=1, Gain=1; REF=AVDD
	-0.3		AVDD+0.3	V	REF2VDD=1, Gain=2/3， REF=AVDD, limited by IO diode clamp
The differential signal is usually the signal output from the OPA inside the chip to the ADC; The single-ended signal is usually the sampled signal from the external input through IO. Whether using an internal/external reference, the signal amplitude should not exceed ±98% of the ADC signal range. In particular, when using an external reference, it is recommended that the sampled signal not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	100k			Ohm	
Input Capacitance		10pF		F	
Reference Voltage (REF)					
Power Supply	2.2	5	5.5	V	
Output Deviation	-9		9	mV	
Rejection Ratio of Power Supply		70		dB	
Temperature Coefficient		20		ppm/°C	
Output Voltage		1.2		V	
Digital-to-Analog Converter (DAC)					

Parameter	Min.	Normal	Max.	Unit	Description
Power Supply	2.2	5	5.5	V	
Load Resistance	5k			Ohm	Output BUFFER is on
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational Amplifier (OPA)					
Power Supply	2.8	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load Resistance	20k			Ohm	
Load Capacitance			5p	F	
Input Common Mode Voltage Range (VICM)	0		AVDD	V	
Output Signal Range	0		2*Vcm	V	Under minimum load resistance
OFFSET		10	15.0	mV	200K:10.4K amplify gain
		10	16.5	mV	190K:20.4K amplify gain
		10	18.5	mV	180K:30.4K amplify gain
		10	20.5	mV	170K:40.4K amplify gain
This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is OPA magnification x OFFSET. The Flash NVR area records the OPA offset for factory tests.					
Common Mode Voltage (Vcm)	1.65	1.9	2.2	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".
Common Mode Rejection Ratio (CMRR)		80		dB	
Power Supply Rejection		80		dB	

Parameter	Min.	Normal	Max.	Unit	Description
Ratio (PSRR)					
Load Current			500	uA	
Slew Rate		5		V/us	
Phase Margin (PM)		60		Degree	
Comparator (CMP)					
Power Supply	2.2	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET		5	10	mV	
Delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'

Table 6-2 LKS32MC088KU8Q8(B) 5V LDO Module Parameter

5V LDO					
Input power	7		20	V	
Output voltage	4.75	5	5.25	V	+/-5% accuracy
Dropout voltage		2		V	
Output current		80		mA	
Ripple rejection		80		dB	
Decoupling capacitor input		0.33		uF	It is added to the VCCLDO pin. Please refer to the pin description section for details
Decoupling capacitor output		1		uF	It is added to the AVDD pin. Please refer to the pin description section for details
Operating temperature range	-40		125	℃	

Description of Analog Register Table:

Address space of 0x40000040 to 0x40000050 are the calibration registers of each analog module. These registers will be set to a unique calibration value in factory. Generally, users are advised not to configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x40000020 to 0x4000003c are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers could be configured in situations.

7 Power Management System

AVDD Power System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

AVDD is powered by a 2.2V ~ 5.5V supply(The B-version chip is powered by 3.0V~5.5V), and all internal digital circuits and PLL modules are powered by an internal LDO15.

The LDO15 is automatically turned on after power-on. No software configuration is necessary. And the LDO15 output voltage can be adjusted by software.

LDO15 has been calibrated before it leaves the factory.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.1V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation.

The PVD module monitors the 5V input power. If it is below a certain threshold, it will remind the MCU by sending an alarm (interrupt) signal. The interrupt reminder threshold can be set to different voltages through the PVDSEL<1:0> registers. The PVD module can be turned off by setting PD_PDT = '1'. For the corresponding value of specific register, please refer to the analog register table.

VCC Power System

The operating power supply voltage range of VCC is 4.5 ~ 20V, which provides power for the on-chip gate driver module. If this voltage is below 4V it will be considered as undervoltage.

8 Clock System

The clock system consists of a 32KHz RC oscillator, a 4MHz RC oscillator, an external 4MHz crystal oscillator, and a PLL.

The 32K RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode; The 4MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz; The external 4MHz crystal oscillator is used as a backup clock.

Both 32k and 4M RC clocks will been through factory calibration. In the range of -40 ~ 105 °C, the accuracy of the 32K RC clock is ± 50%, and the accuracy of the 4M RC clock is ± 1%.

The 4M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 4M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 4M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and could be enabled by software.

The crystal oscillator circuit has a built-in amplifier and an oscillator capacitor. Connect a crystal between IO OSC_IN/OSC_OUT and set XTALPDN = ’1’ to start the oscillation.

9 Reference Voltage

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = ’0’. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

The voltage reference can be measured by setting REF_AD_EN = ’1’ and via IO P2.3.

10 Analog Digital Converter

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 4M RC clock and PLL should be turned on first. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

The synchronous double sampling circuit can sample the two input analog signals at the same time. After the sampling is completed, the ADC converts the two signals one by one and writes them into the corresponding data registers.

ADC takes 16 ADC clock cycles to complete one conversion, of which 13 are conversion cycles and 3 are sampling cycles. I.E. $f_{conv}=f_{adc}/16$. When the ADC clock is set to 48MHz, the conversion rate is 3Msps.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, One-time 1 to 20 channels scanning mode, continuous 1 to 20 channels scanning mode. It has a set of 20 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

Among the 20 analog channels, the 19th channel is analog ground and is used to measure the offset of the ADC. The ADC values of other channels will be automatically subtracted by this offset. The offset is calibrated in factory and store in flash. Each time the chip is powered up, this offset will be loaded into ADC_DC register automatically. If the user needs to improve the offset over the whole temperature, it can be recalculated time by time (for example, each hour) when the ADC is idle.

When GAIN_REF = 0, the ADC voltage reference is 2.4V. The ADC has two gain modes, which are set by GAIN_SHAx, corresponding to 1x and 2/3 x gain setting; 1x gain corresponds to an input signal range of ± 2.4V, and 2/3 gain corresponds to an input signal range of ± 3.6V. When measuring the output signal of the OPA, select the specific ADC gain according to the maximum signal that the OPA may output.

11 Operational Amplifier

4-channel of rail-to-rail OPAs (3 channels for 084D) are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 4-channels amplifiers by setting OPAOUT_EN <2:0>, and send it to the P2.7 IO port through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description"). Because of this buffer, the OPA is able to be output to an IO while operating normally.

When the chip is powered on, the OPA module is OFF by default. It can be turned on by setting OPAxPDN = ’1’, and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 2-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay can be set to 0.15uS/0.6uS by register IT_CMP. and the hysteresis voltage can be set to 20mV/0mV by CMP_HYS.

The signal sources of the positive and negative inputs can be programmed by register CMP_SELP<2:0> and CMP_SELN<1:0>. For details, please refer to the analog register description.

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = '1', and turn on the BGP module before turning on the comparator.

13 Temperature Sensor

The chip has a temperature sensor with an accuracy of ±2°C in -40~85℃ and ±3°C in -40~105℃ typically. The temperature sensor will be calibrated in factory, and the calibration value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1', and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 Digital Analog Converter

The chip has a 1-channel 12bit DAC, the maximum range of the output signal can be set to 1.2V/3V/4.85V through the register DAC_GAIN <1:0>.

The 12bit DAC can be output via IO port P0.0 by setting register DACOUT_EN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output data rate of the DAC is 1Msps.

When the chip is powered on, the DAC module is OFF by default. DAC can be turned on by setting DAC12BPDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor

- 32-bit Cortex-M0 + DSP dual-core processor
- Two-wire SWD debug pin
- System frequency is up to 96MHz

16 Storage

16.1 Flash

- built-in flash including 32kB/64kB main area and 1kB NVR
- Endurance: 20,000 Cycles(min)
- Data retention: more than 100 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size 512bytes, supporting Sector erase/program and in-application program
- Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF

16.2 SRAM

- built-in 8kB SRAM

17 Motor Control PWM

- MCPWM operating frequency is up to 96MHz
- Supports up to 4 channels of complementary PWM output with adjustable phase
- The width of dead-zone in each channel can be configured independently
- Support edge-aligned PWM
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simutaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support capture mode for measuring external signal/pulse width
- Support comparison mode for timed interruption of edge-aligned PWM

19 Hall Sensor Interface

- Built-in 1024 cycles filtering
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 DSP

- Customized DSP instruction set for motor control algorithm, , three-stage pipeline achitecture
- Operating frequency is up to 96MHz
- 32/16-bit divider, could finish one division calculation in 10 cycles
- 32-bit hardware SQRT, could finish one SQRT calculation in 8 cycles
- Q15 format Cordic trigonometric function module, could finish sin/cos/artanc calculation in 8 cycles
- DSP has independent program memory and data memory, DSP could execute its program independently, and can also be called by MCU to perform a certain calculation as a AHB slave like a coprocessor
- Support DSP IRQ and pause state for data exchange purpose with MCU

21 General Peripherals

- Two UART, full-duplex operation, support 7/8 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- One CAN-bus (084D without CAN)
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, with write protection and 2/4/8/64 seconds reset interval.

22 Gate Driver Module

22.1 Module Parameter

The internal gate driver module of the chip has 5 different parameter specifications. According to the different gate driver circuit parameters, the gate driver module is divided into 5 models, which are G1~G5 respectively. The comparison table is as Table 22-1.

Table 22-1 Device-Gate driver circuit version comparison table

Device	Date Code	Gate Driver
LKS32MC084DF6Q8(B)	YYWWB	G2
	YYWWXE	G6
LKS32MC086N8Q8(B)	YYWWXC	G2
LKS32MC088KU8Q8(B)	YYWWX	G5
LKS32MC088K22U8Q8	YYWWX	G7

"YYWWX*" is the data code and chip version number, see the third line of the chip silk print. "YYWWX" is the production date, "*" is optional, and is usually A, B, C, D... or blank, which represents the version number of the chip pre-driver.

22.1.1 Gate Driver Module G1/Gate Driver Module G4

Table 22-2 Gate Driver Module G1/Gate Driver Module G4 parameter

Parameter	Min	Typ	Max	Unit	Description
Absolute Maximum Ratings					
Low side and logic fixed supply VCC	-0.3		+25.0	V	To ground
High side floating supply VB	-0.3		+300	V	
High side offset VS	VB-25		VB+0.3	V	
High side output $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low side output $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	Lower of +15V or VCC+0.3
Allowable offset voltage slew rate dVs/dt			50	V/ns	
Package power dissipation Pd			1.6	W	Room temperature 25°
Thermal resistance R_{thJA}			83	℃ /W	
Junction temperature TJ			150	℃	
Storage temperature Ts	-55		150	℃	
Lead temperature			300	℃	Soldering for 10s
Recommended Operating Conditions					

Low side and logic fixed supply VCC	+4.5		+20	V	To ground
High side floating supply VB	VS+4.5		VS+20	V	
High side offset VS	0		260	V	
High side output $HO_{1,2,3}$	VS		VB	V	
Low side output $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		5	V	
Ambient temperature T_A	-40		125	℃	
Gate driver Electrical Characteristic					
VCC supply under-voltage trigger voltage	2.9	4.2	5.5	V	
Quiescent VCC supply current	210	330	450	uA	Vin =0V or5V
Quiescent VBS supply current	25	45	65		Vin =0Vor5V
High side bias leakage current	—	—	10	uA	VB =VS =260V
High side output HIGH short-circuit pulse current	1200	1500	—	mA	VO = 0V, VIN = VIH PW 10 us
High side output LOW short-circuit pulse current	1200	1500	—		VO = 15V, VIN = VIL PW 10 us
Turn-on propagation delay T_{on}	—	220	260	ns	VS = 0V
Turn-off propagation delay T_{off}	—	110	140		VS = 0V
Turn-on rise time T_r	—	37	—		C_L=1nF
Turn-off fall time T_f	—	30	—		
Dead time D_T	—	100	—		
Delay matching M_T	—	—	50		

[1]YYWW is date code on chip package

22.1.2 Gate Driver Module G2

Table 22-3 Gate Driver Module G2 parameter

Parameter	Min	Typ	Max	Unit	Description
Absolute Maximum Ratings					
Low side and logic fixed supply VCC	-0.3		+25.0	V	To ground
High side floating supply VB	-0.3		+250	V	
High side offset VS	VB-25		VB+0.3	V	
High side output $HO_{1,2,3}$	VS-0.3		VB+0.3	V	

Low side output $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Allowable offset voltage slew rate dVs/dt			50	V/ns	
Junction temperature TJ	-40		150	℃	
Storage temperature Ts	-55		150	℃	
Lead temperature			300	℃	Soldering for 10s
Recommended Operating Conditions					
Low side and logic fixed supply VCC	+8		+20.0	V	相对于地
High side floating supply VB	VS+8		VS+20	V	
High side offset VS	-5		200	V	
High side output $HO_{1,2,3}$	VS		VB	V	
Low side output $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	
Ambient temperature T_A	-40		125	℃	
Gate driver Electrical Characteristic					
Quiescent VCC supply current		50	100	uA	HIN=LIN=0V
Quiescent VBS supply current		20	40	uA	HIN=LIN=0V
Floating supply leakage I_{LK}			10	uA	VB=VS=220V
VCC supply under-voltage trigger voltage	4.0	4.7	6.7	V	
VBS supply under-voltage trigger voltage	3.9	5.6	6.9	V	
VCC supply under-voltage lock -on voltage	3.6	4.4	6.4	V	
VBS supply under-voltage lock -on voltage	3.5	5.0	6.2	V	
VCC supply under-voltage hysteresis voltage	0.25	0.3	0.8	V	
VBS supply under-voltage hysteresis voltage	0.25	0.6	0.8	V	
High level input threshold voltage V_{IH}	2.8			V	
Low level input threshold voltage V_{IL}			0.8	V	
Input bias current I_{source}		32	120	uA	HIN=LIN=5V
Input bias current I_{sink}			1	uA	HIN=LIN=0V
High level output, $V_{BIAS}-V_O$			1	V	I_O=20mA
Low level output, V_O			1	V	I_O=20mA

High level output short current I_{O+}	650	1000		mA	V_{CC}/V_{BS}=15V
Low level output short current I_{O-}	650	1000		mA	V_{CC}/V_{BS}=15V
Turn-on propagation delay T_{on}		270	500	ns	
Turn-off propagation delay T_{off}		80	150	ns	
Turn-on rise time T_r		15	30	ns	C_L=1nF
Turn-off fall time T_f		12	30	ns	
Dead time D_T	100	200	400	ns	
Delay matching M_T			80	ns	T_{on} & T_{off} for (HS-LS)

22.1.3 Gate Driver Module G3

A bootstrap diode is integrated in the pre-driver.

Table 22-4 Gate Driver Module G3 parameter

Parameter	Min	Typ	Max	Unit	Description
Absolute Maximum Ratings					
Low side and logic fixed supply VCC	-0.3		+25.0	V	To ground
High side floating supply VB	-0.3		+250	V	
High side offset VS	VB-25		VB+0.3	V	
High side output $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low side output $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Allowable offset voltage slew rate dVs/dt			50	V/ns	
Junction temperature TJ	-40		150	°C	
Storage temperature Ts	-55		150	°C	
Lead temperature			300	°C	Soldering for 10s
Recommended Operating Conditions					
Low side and logic fixed supply VCC	+4.5		+20.0	V	To ground
High side floating supply VB	VS+10		VS+20	V	
High side offset VS	-5		200	V	
High side output $HO_{1,2,3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low side output $LO_{1,2,3}$	0		VCC	V	

Logic input HIN/LIN$_{1,2,3}$	0		5	V	
Ambient temperature T_A	-40		125	℃	
Gate driver Electrical Characteristic					
Quiescent VCC supply current1	210	330	450	uA	HIN=LIN=0/5V, ENB=0
Quiescent VCC supply current2		46	80	uA	HIN=LIN=0/5V, ENB=5
Quiescent VBS supply current	25	45	65	uA	HIN=LIN=0V
Floating supply leakage I_{LK}			10	uA	VB=VS=220V, VCC=0V
Driving Current I_{O+}		1		A	
Driving Current I_{O-}		1.2		A	
VCC supply under-voltage positive going threshold	2.9	4.2	5.5	V	
VCC supply under-voltage negative going threshold	2.5	3.8	5.1	V	
VCC supply under-voltage lockout hysteresis		0.4		V	
VBS supply under-voltage positive going threshold	2.5	3.8	4.5	V	
VBS supply under-voltage negative going threshold	2.2	3.5	4.5	V	
VBS supply under-voltage lockout hysteresis		0.3		V	
High level input threshold voltage V_{IH}	2.5			V	
Low level input threshold voltage V_{IL}			0.8	V	
Turn-on rise time T_r		27		ns	C_L=1nF
Turn-off fall time T_f		20		ns	
Turn-on propagation delay T_{on}		600	700	ns	
Turn-off propagation delay T_{off}		280	400	ns	
Dead time D_T	220	280	330	ns	
Delay matching M_T			60	ns	

22.1.4 Gate Driver Module G5

Table 22-4 Gate Driver Module G5 parameter

Parameter	Min	Typ	Max	Unit	Description
Absolute Maximum Ratings					

Low side and logic fixed supply VCC	-0.3		+25.0	V	To ground
High side floating supply VB	-0.3		+625	V	
High side offset VS	VB-25		VB+0.3	V	
High side output $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low side output $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Allowable offset voltage slew rate dVs/dt			50	V/ns	
Junction temperature TJ	-40		150	℃	
Storage temperature Ts	-55		150	℃	
Thermal resistance θJA			200	℃/W	junction to ambient
Recommended Operating Conditions					
Low side and logic fixed supply VCC	+10		+20.0	V	To ground
High side floating supply VB	VS+10		VS+20	V	
High side offset VS	-5		600	V	
High side output $HO_{1,2,3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low side output $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	
Gate driver Electrical Characteristic					
Quiescent VCC supply currentI_{QCC}		50	150	uA	HIN=LIN=0V
Quiescent VBS supply currentI_{QBS}		35	80	uA	HIN=LIN=0V
Offset supply leakage currentI_{LK}			10	uA	VHO=VB=VS=620V
VCC under voltage rising threshold	8	8.5	9.8	V	
VBS under voltage rising threshold		8.7	10	V	
VCC under voltage falling threshold	7.2	7.6	8.8	V	
VBS under voltage falling threshold	6.5	7.8		V	
VCC under voltage hysteresis voltage	0.6	0.9	1.2	V	
VBSunder voltage hysteresis voltage		0.9		V	
High level output voltage V_{IH}	2.4			V	

Low level output voltage V_{IL}			0.6	V	
Logic 1 Input bias current I_{source}		32	100	uA	HIN=LIN=5V
Logic 0 Input bias current I_{sink}			1	uA	HIN=LIN=0V
High level output voltage V_{OH}			1	V	I_O=20mA
Low level output voltage, V_{OL}			1	V	I_O=20mA
Output high short circuit pulse current I_{O+}	300	450		mA	VO=0V, VIN=5V,Pulse Width < 10uS
Output low short circuit pulse current I_{O-}	650	1000		mA	VO=15V, VIN=0V,Pulse Width < 10uS
Turn-on rise time T_r		15	30	ns	C_L=1nF
Turn-off fall time T_f		12	30	ns	
Turn-on propagation delay T_{on}	100	250	450	ns	VS=0V
Turn-off fall time T_{off}	80	160	300	ns	VS=0V or 600V
Dead time D_T	40	100	250	ns	
Delay match M_T			80	ns	T_{on} & T_{off} for (HS-LS)

22.1.5 Gate Drive Module G6

Table 22-5 Parameter of Gate Drive Module G6

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+22.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	-0.3		+60	V	034S2 $VB_{1,2,3Max}$=250V
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					

Supply voltage VCC	+7.0		+20.0	V	Relative to ground
Floating voltage $VB_{1, 2, 3}$	VS+8		VS+20	V	
Floating bias $VS_{1, 2, 3}$	-5		60	V	034S2 $VS_{1, 2, 3Max}$=200V
High-side output voltage $HO_{1, 2, 3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low-side output voltage $LO_{1, 2, 3}$	0		VCC	V	
Logic input $HIN/LIN_{1, 2, 3}$	0		5	V	
Operating temperature T_A	-40		125	℃	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC}		110		uA	HIN=LIN=0/5V
VB static current I_{QBS}		25	50	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			10	uA	VB=VS=200V, VCC=0V
drive current I_{O+}	0.65	1		A	
drive current I_{O-}	0.65	1		A	
VCC undervoltage rising edge trigger voltage	3.5	4.2	4.9	V	
VCC undervoltage falling edge trigger voltage	3.2	3.8	4.8	V	
VCC undervoltage lockout hysteresis	0.25	0.4	0.8	V	
VBS undervoltage rising edge trigger voltage	2.5	3.8	5.5	V	
VBS undervoltage falling edge trigger voltage	2.2	3.5	4.8	V	
VBS undervoltage lockout hysteresis	0.25	0.3	0.8	V	
High input threshold V_{IH}	2.8			V	
Low input threshold V_{IL}			0.8	V	
Output rise time T_r		20	30	ns	C_L=1nF
Output fall time T_f		12	30	ns	
Turn-on delay time T_{on}		250	500	ns	
Shutdown delay time T_{off}		120	200	ns	
Dead zone D_T	50	150	400	ns	
Delay matching M_T			80	ns	

22.1.6 Gate Drive Module G7

* The FO signal of the gate drive module is internally connected to the chip pin P2.8

Table 22-6 Parameter of Gate Drive Module G7

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+25.0	V	Relative to ground

Floating voltage $VB_{1,2,3}$	-0.3		+650	V	
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	°C	
Storage temperature (TS)	-55		150	°C	
Welding temperature			300	°C	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+13		+20.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	VS+13		VS+20	V	
Floating bias $VS_{1,2,3}$	-5		600	V	
High-side output voltage $HO_{1,2,3}$	VS		VB	V	
Low-side output voltage $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	
Operating temperature T_A	-40		105	°C	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC}			2300	uA	HIN=LIN=0V
VB static current I_{QBS}			100	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			50	uA	VB=VS=620V
VCC supply under-voltage trigger voltage	11	12	12.8	V	
VCC supply under-voltage lock -on voltage	9.5	10.4	11	V	
VCC supply under-voltage hysteresis voltage	1	1.6	2	V	
High input threshold V_{IH}	1.7		2.4	V	
Low input threshold V_{IL}	0.8	1.0	1.2	V	
High level output short current I_{O+}	115	200		mA	
Low level output short current I_{O-}	250	350		mA	
Short circuit trip level V_{CIN_REF}	0.455	0.48	0.505	V	VCC=15V
Fault output voltage V_{FOL}			0.95	V	
Fault output pulse width t_{FO}	20	65		us	
Output rise time T_r		65		ns	C_L=1nF
Output fall time T_f		25		ns	
Turn-on delay time T_{on}	350	500	700	ns	
Shutdown delay time T_{off}	350	500	700	ns	
Delay matching M_T			60	ns	T_{on} & T_{off} for (HS-LS)
CIN detection input filter time $T_{FLT-CIN}$	100	300	500	ns	CIN 0->1V, test CIN rising edge to LO falling edge delay

22.2 Recommended Application Diagram

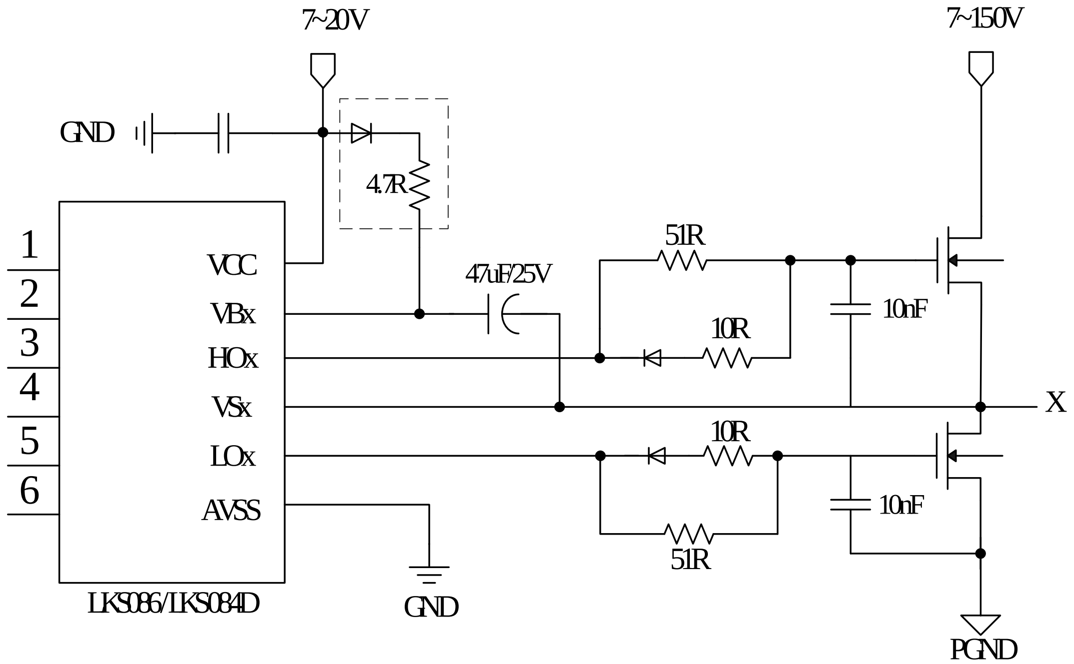

Fig. 22-1 Gate Driver Module G1/G2/G4/G5 Application Diagram

It's recommended to add bootstrap diode between VBx and VCC for G1/G2/G4/G5.

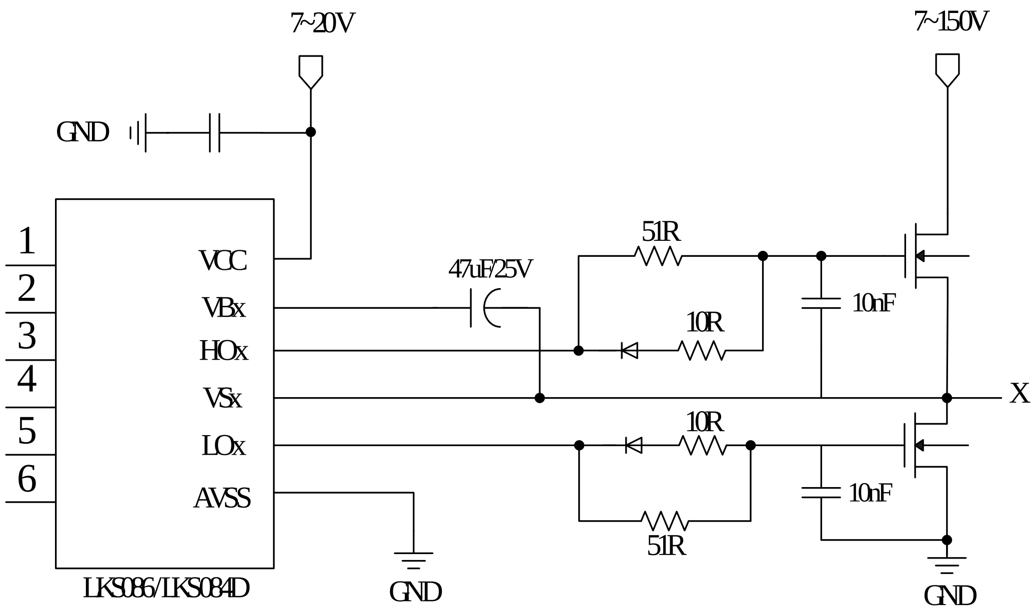

Fig. 22-2 Gate Driver Module G3 Application Diagram

Gate Driver Module G3 has built-in bootstrap diode, so the bootstrap on board won't be necessary. But you could still use a bootstrap diode for compatibility concern.

Only the gate drive module pins are shown in the figure, where x = 1,2,3 corresponding to the three sets of MOS gate drive outputs. The application diagram of each set is shown in Fig. 22-1 and Fig. 22-2.

Table 22-7 Gate Driver Module LIN/HIN V.S. MCU Pin

Gate Driver Input	G1/2/3/4	G5	Note
LIN0		P1.5	P3.13 should be output enabled
HIN0		P1.4	
LIN1	P1.5	P1.7	P3.13 should be output enabled
HIN1	P1.4	P1.6	
LIN2	P1.7	P1.9	P1.12 should be output enabled
HIN2	P1.6	P1.8	
LIN3	P1.9		P1.15 should be output enabled
HIN3	P1.8		

Gate driver input-output transfer function:

Table 22-8 Gate Driver Module G1/G2/G3/G5 truth table

{HIN,LIN}	HO	LO	
00	0	0	Low side and high side are all off
01	0	1	Low side on
10	1	0	High side on
11	0	0	Low side and high side are all on, which will trigger short protection

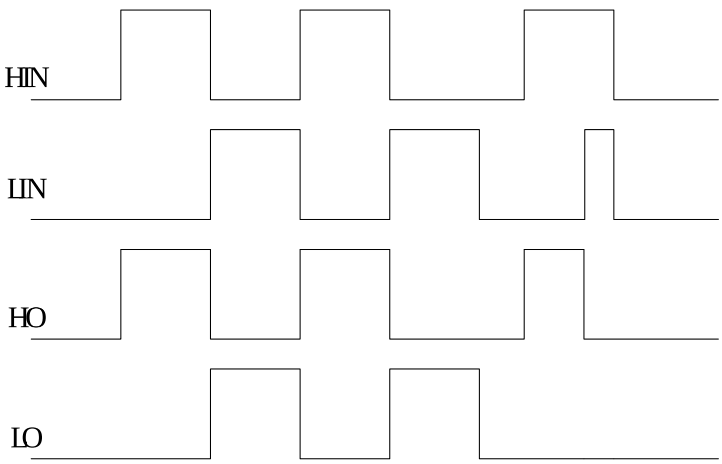

Fig. 22-3 Gate Driver Module G1/G2/G3/G5 polarity illustration

Table 22-9 Gate Driver Module G4 Gate driver truth table

{HIN,$\overline{\text{LIN}}$}	HO	LO	
00	0	1	Low side on
01	0	0	Low side and high side are all off
10	0	0	Low side and high side are all on, which will trigger short protection
11	1	0	High side on

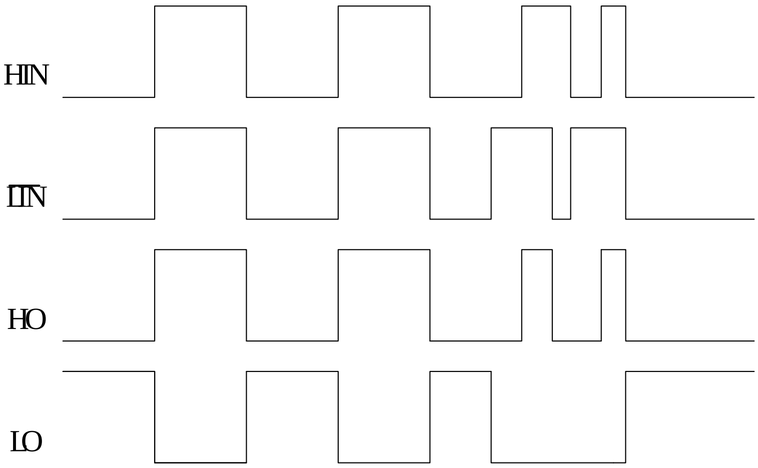

Fig. 22-4 Gate Driver Module G4 polarity illustration

23 Special IO Multiplexing

Notes for Special IO Multiplexing of LKS08x

The SWD protocol includes two signals: SWCLK and SWDIO. SWCLK is a clock signal. To the chip, it is an input and will always be an input. SWDIO is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Users could use two IOs of SWD as GPIOs P0.0/P2.15. The precautions are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.
- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In SSOP24 package and QFN40 package, SWDIO is directly bonded with P0.0 and P2.15, and the corresponding GPIO can be directly enabled. It is recommended that SWDCLK keep unchanged (constant 1 or constant 0) when multiplexing SWDIO

For LKS087E, SWDCLK is bonded with P2.6 and the corresponding GPIO can be directly enabled. If SWDIO and SWDCLK are multiplexed at the same time, considerations for SWDCLK multiplexing are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability

of the successful one-time erasion.

- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

When SWDCLK and SWDIO pins are used as GPIO, they should not act at the same time. That is, when SWDCLK multiplexing is enabled and changes, SWDIO can remain at level 0 (similar to time division multiplexing).

For RSTN signal, the default is for the external reset pin of LKS08x chip.

LKS08x allow users to multiplex RSTN as other IOs, and the multiplexed IO is P0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

24 Ordering Information

The package type is divided into Tray package and Reel package. The number of chips in the specific package is determined by the package form and package type, and is no longer distinguished by the chip model.

Tray packaging information is shown in the table below

Packaging form	Quantity per plate /tube	Number of inner boxes	Number of outer boxes
SOP16/ESOP16L	3000/plate	6000PCS	48000PCS
SSOP24	4000/plate	8000PCS	64000PCS
SSOP24	50/tube	10000PCS	4000/100000PCS
QFN 8*8	260/plate	2600PCS	15600PCS
QFN 4*4/5*5/6*6	490/plate	4900PCS	29400PCS
QFN 3*3	5000/plate	5000PCS	40000PCS
LQFP48/TQFP48 0707	250/plate	2500PCS	15000PCS
LQFP64 1010	160/plate	1600PCS	9600PCS
LQFP100 1414	90/plate	900PCS	5400PCS
TSSOP20/28	4000/plate	8000PCS	64000PCS

Reel packaging information is shown in the table below

Packing category		Quantity per plate /tube	Quantity per box	Number of boxes per carton	Number of outer boxes
Braid-13 inch	SOP/ESOP8	4000	8000	8	64000
Braid-13 inch	SOP/ESOP16	3000	6000	8	48000
Braid-13 inch	SSOP24	4000	8000	8	64000
Braid-13 inch	TSSOP20	4000	8000	8	64000
Braid-13 inch	D/QFN3*3	5000	10000	8	80000
Braid-13 inch	D/QFN4*4	5000	10000	8	80000
Braid-13 inch	D/QFN5*5	5000	10000	8	80000
Tube installation	SOP16	50	10000	10	100000
Tube installation	SOP14/SSOP24	50	10000	10	100000
Tube installation	TSSOP24	54	6480	6	38880

25 Version History

Table 25-1 Document's Version History

Date	Version No.	Description
2025.07.21	1.88	Delete the Flash section: erase/program one sector while accessing another
2025.07.10	1.87	Analog performance parameters add operational amplifier OFFSET parameter description correction
2025.07.09	1.86	Original 088K2U8Q8 is updated to 088K22U8Q8, FO pin information is modified Add the OFFSET parameter of the operational amplifier to the simulation performance parameter
2024.12.12	1.85	Description of Added ADC Saturation Range
2024.08.28	1.84	088K2U8Q8 Pin assignment modified
2024.08.15	1.83	Delete specific pre-drive silkscreen Add 088K2U8Q8
2024.08.06	1.82	Order package information update to confirm package information by package type and package form
2024.03.13	1.81	084D Added models with G6 predrive
2024.01.26	1.80	Modified device selection guide
2023.12.12	1.79	Added description of pull-up resistance values
2023.11.09	1.78	OPA OFFSET Adds the description, Renewal storage temperature
2023.08.24	1.77	Revise the Date Code of 084D
2023.05.28	1.76	Add 5V LDO parameter of 088K
2023.04.28	1.75	Add B-version chip with AVDD power supply range of 3.0-5.5V Modify Package Name
2023.04.03	1.74	Revise the pin function description of LKS32MC086N8Q8
2023.04.03	1.73	Adjust AVDD range from 2.2~5.5 to 3.0~5.5V
2023.03.24	1.72	Update QFN40(084D) package dimension
2023.03.18	1.71	Modified the description of clock accuracy
2023.01.13	1.7	Add ordering information
2022.12.12	1.69	Revise the pin function description of LKS32MC086N8Q8
2022.11.30	1.68	Revise gate driver module G1 parameter.
2022.11.19	1.67	Revise date driver parameter description.
2022.11.15	1.66	Revise special IO Multiplexing
2022.11.08	1.65	Add description of 088K gate driver polarity
2022.11.07	1.64	Add connection resistance between IO and internal analog circuit
2022.10.28	1.63	Add characteristic of common mode voltage
2022.10.13	1.62	Revise 088K pin assignment
2022.08.04	1.61	Add 088K
2021.12.30	1.6	Revise gate driver description
2021.04.13	1.5	The whole family device selection guide

2020.09.19	1.4	Minor revision
2020.07.10	1.3	Revise gate drive module parameter
2020.03.19	1.2	Add gate drive module
2019.07.18	1.1	Revise 084D's definition
2019.03.10	1.0	Initial version

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