Linko Semiconductor Co., Ltd.

LKS32MC08x with built-in 3P3N driver Datasheet

1 Overview

1.1 Function

LKS32MC087D/EM6S8(B) are 32-bit MCU targeting motor control applications. With all modules required for common motor control systems and three-phase P/N MOS gate driver, it can directly drive three-channel P/N MOS power device.

- **Features**
  - 96MHz 32-bit RISC core
  - Low power sleep mode
  - Integrated three-phase P/N MOS gate driver
  - Industrial temperature range
  - High ESD and group pulse reliability
- **Memory**
  - 32kB Flash with optional encryption and 128-bit chip unique identifier
  - 8kB RAM
- **Operating Conditions**
  - 7.5~28V (Maximum: 40V), single power supply, with an integrated internal 5V LDO for partial power supply for internal MCU of chip
  - Operating Conditions: -40~105℃
- **Clock**
  - 4MHz built-in high-precision RC clock, with an accuracy of ± 1% at -40 ~ 105 ℃
  - 32KHz built-in low-speed clock for low-power mode
  - Support External 4MHz crystal oscillator
  - Internal PLL up to 96 MHz clock
- **Peripheral Modules**
  - One UART
  - Two 16-bit timers, support capture and edge-aligned PWM function
  - Two 32-bit timers, support capture and edge-aligned PWM function;
  - Motor control PWM module, supports 6 channels of PWM output, independent dead-band control
  - Hall signal interface with speed measurement and debouncing function
  - Hardware watchdog
  - 4 Groups of 16bit GPIO, among which P0.0/P0.1/P1.0/P1.1 could be used as wakeup signals. P0[15:0] could be used as external IRQ.

- **Analog Modules**
  - Integrated one 12-bit SAR ADC, 2Msps sampling and conversion rate, 16 channels in total
  - Integrated 2 operational amplifiers, differential PGA mode available
  - Integrated two comparators with hysteresis
  - Integrated 12-bit DAC digital-to-analog converter
  - ± 2 ℃ built-in temperature sensor
  - Built-in 1.2V 0.8% precision voltage reference source
  - Built-in one low-power LDO and power monitoring circuit
  - Integrated RC clock with high precision and low temperature drift
  - Crystal oscillator circuit
  - Integrated 32kHz+4MHz RC
  - Integrated 96MHz PLL

- **Packaging:**

Table 1-1 Packaging summary Table for LKS32MC08x with Built-in 3P3N Driver

Device	Package
LKS32MC087DM6S8(B)	SSOP24L
LKS32MC087EM6S8(B)	SSOP24L

1.2 Main Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 2 channels high-speed OPAs and 2 channels comparators, meeting the different needs of single resistance/double resistance current sampling topology structure;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be directly input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed high current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Single power 7.5~28V supply, integrated 5V LDO internally;
- The three-phase P/N MOS gate driver is integrated;
- Supports IEC/UL60730 functional safety certification;

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC / non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Conventions

LKS32 MC 080 R 8 T 8 XX （X）

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

080/081/082/ 083/085/088	= 2.2~5.5V,1 ADC,4 PGA,DSP
084D/086	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver
087(A)	= 2.2~5.5V,1 ADC,2 PGA
087C	= 2.2~5.5V,1 ADC,2 PGA, CAN
087D/087E	= 7.5~28V, 1 ADC,2 PGA,3P3N Driver
089	= 2.2~5.5V,1 ADC,2 PGA
089XL	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver,LIN

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Options

TR	= Tape and reel packing
P	= Engineering Samples

Version

X	= Version, B~Z

Fig. 1-1 Naming Conventions of LKS32MC08x Components

1.4 System Resource

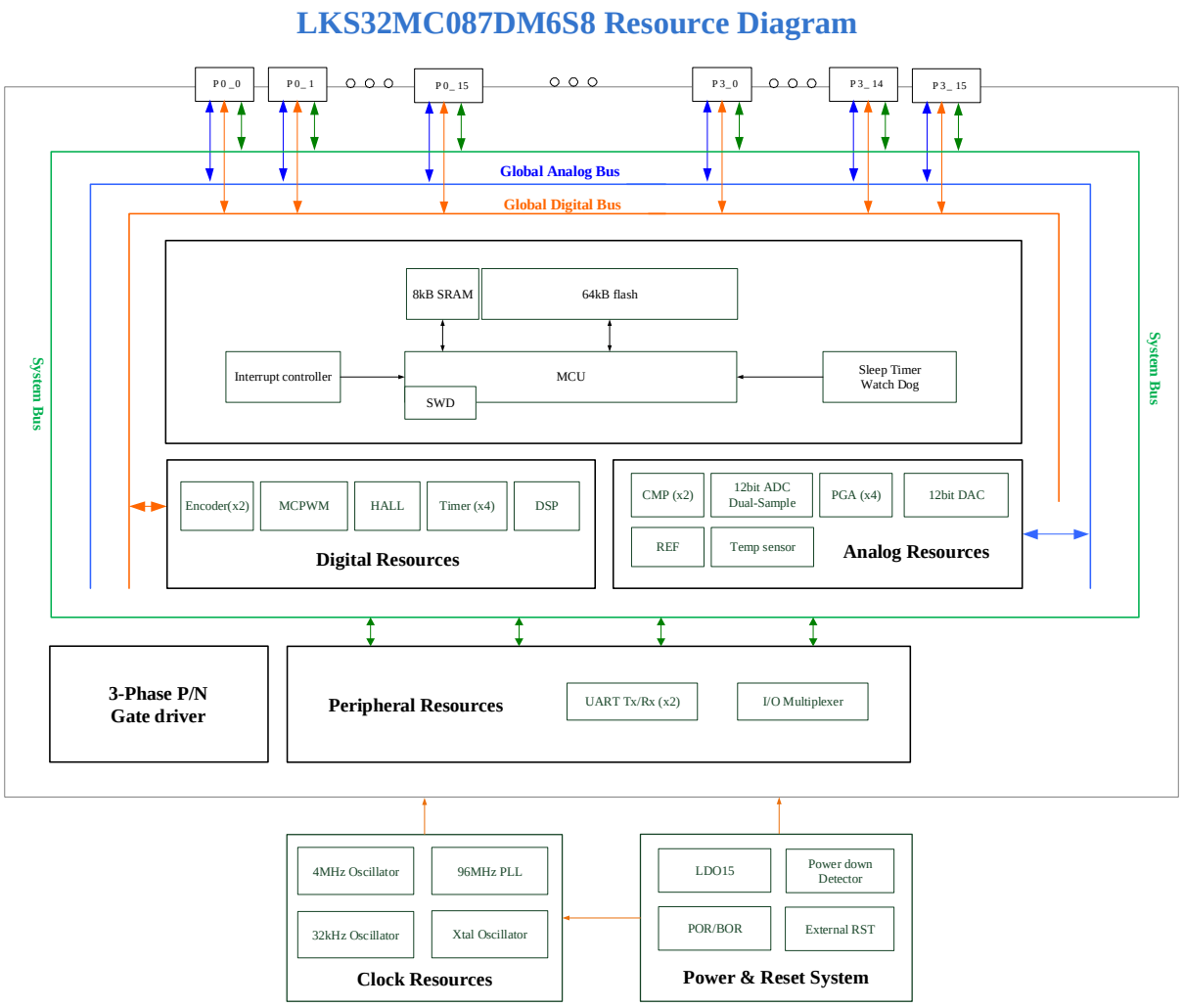

Fig. 1-2 System Block Diagram of LKS32MC08x with Built-in 3P3N Driver

1.5 FOC System Example

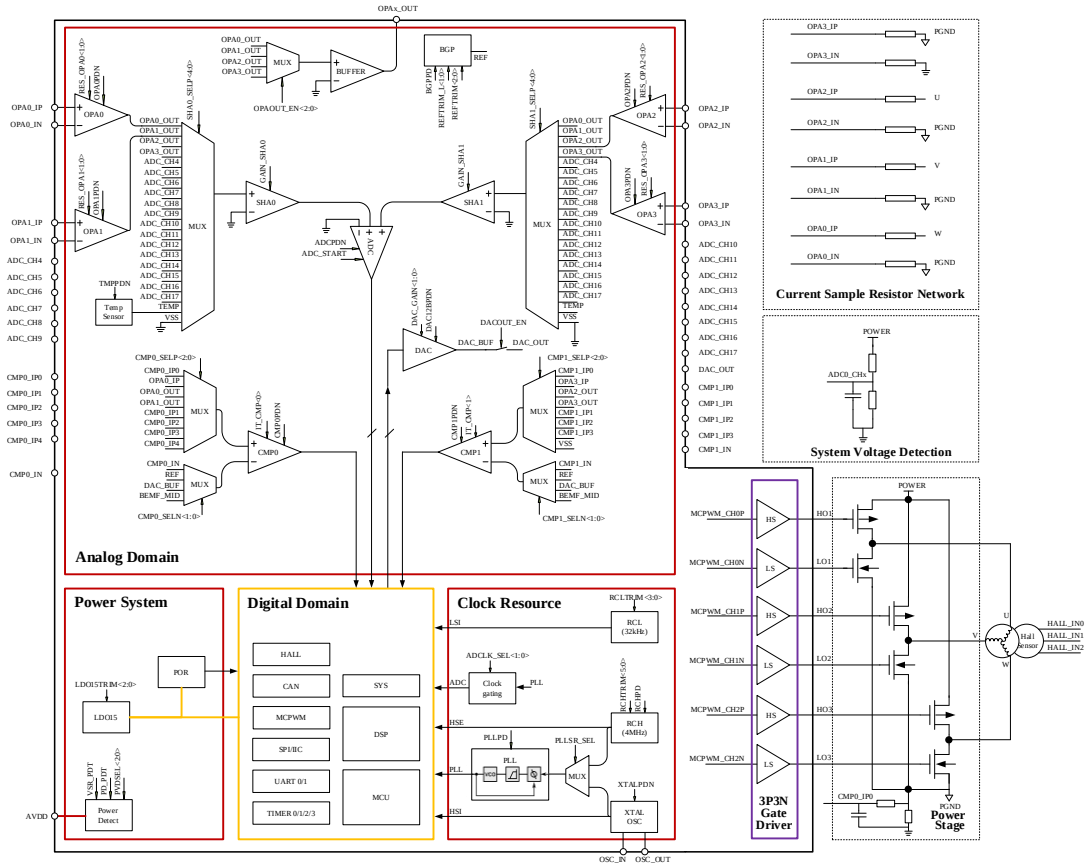

Fig. 1-3 LKS32MC08x with Built-in 3P3N Driver Simplified Schematic of FOC System

2 Device Selection Guide

Table 2-1 LKS08x family device selection guide

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC080R8T8(B)	96	64	8	13	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						LQFP64
LKS32MC081C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC082K8Q8(B)	96	64	8	8	12BITx1	2	6	3	3	1	1	2		Yes	Yes							QFN5*5 32L-0.75
LKS32MC083C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						TQFP48
LKS32MC084DF6Q8	96	32	8	11	12BITx1	2	7	3	3	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20*1	200		QFN5*5 40L-0.75
LKS32AT085C8Q9	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						QFN6*6 48L-0.55
LKS32AT086N8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC086N8Q8	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC087M6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087AM6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087CM8S8(B)	96	64	8	5	12BITx1	2	6	2	3			1	Yes	Yes	Yes							SSOP24L
LKS32MC087DM6S8	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO*2	SSOP24L
LKS32MC087EM6S8	96	32	8	5	12BITx1	2	7	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO	SSOP24L
LKS32MC088C6T8(B)	96	32	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC088KU8Q8	96	64	8	8	12BITx1	2	7	3	3	1	1	2	Yes	Yes	Yes	Yes	6N	+0.45/-1	4.5~20	600	5V LDO	QFN43L
LKS32MC088K2U8Q8	96	64	8	8	12BITx1	2	7	3	3	1	1	2	Yes	Yes	Yes	Yes	6N	+0.45/-1	4.5~20	600	5V LDO	QFN43L
LKS32AT089XLN8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200	5V LDO	QFN6*6 52L-0.55

*1 : Some devices are divided into different versions due to the integration of multiple pre drives. The power supply voltage range of the pre drive is different. Please refer to the electrical performance parameters for details.

*2 : Some devices are equipped with a 5V LDO, which is powered by 7.5~28V VCC and could supply 5V to MCU or peripheral devices. Please refer to Pin as-

signment table for more information.

3 Pin Assignment

3.1 Pin Assignment

3.1.1 Special Notes

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.
SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32MC087DM6S8(B)

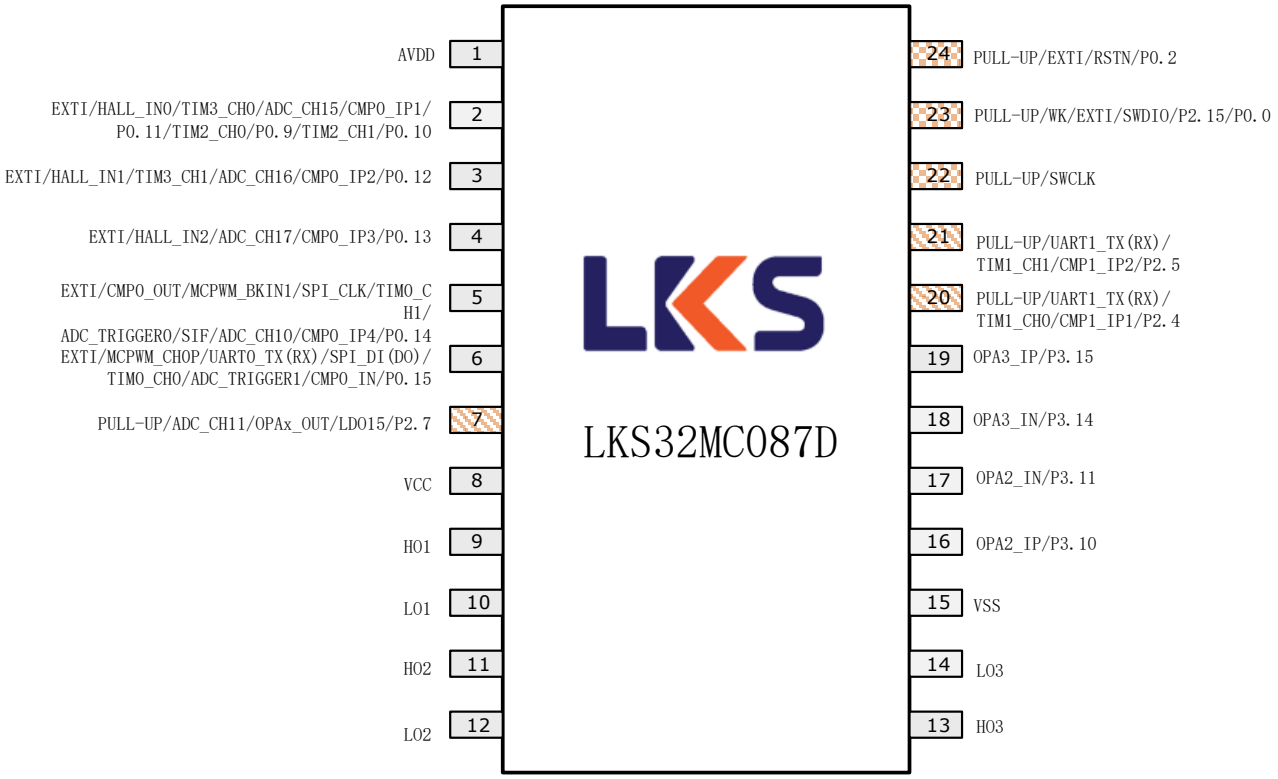

Fig. 3-1 LKS32MC087DM6S8(B) Pin Assignment

3.1.3 LKS32MC087EM6S8(B)

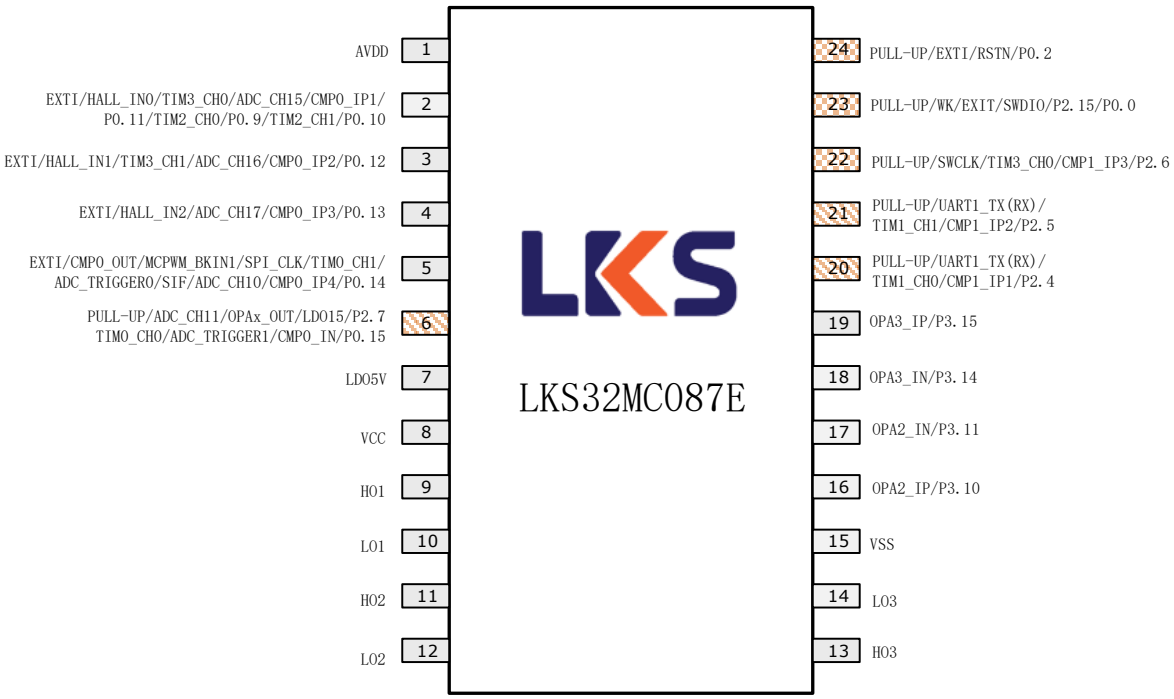

Fig. 3-2 LKS32MC087EM6S8 Pin Assignment

3.2 Pin Function Description

Table 3-1 LKS32MC08x with Built-in 3P3N Driver Pin function

087D	087E	Pin Name	Type	Description
1	1	AVDD	PWR	For 087D, AVDD is 5V LDO output. A 1uF decoupling capacitor is required, and it should be as close as possible to the LDO5V pin. For 087E, AVDD is the low-voltage power supply, power supply range 3.3~5.5V. In applications with good heat dissipation conditions, it can be directly connected to the LDO5V pin of the chip. To reduce the system power consumption and use the 5V power supply generated by an external DCDC or charge pump, connect this pin to the external 5V power supply
2	2	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11/TIM2_CH0/P0.9/TIM2_CH1/P0.10	IO	Hall Sensor A-phase input/Timer3 channel 0/ADC channel 15/Comparator 0 positive input channel 1/P0.11/ Timer2 channel 0/P0.9/ Timer2 channel 1/P0.10 Any two of the three GPIO: P0.11/P0.9/P0.10 should NOT be used as output simutaneously
3	3	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/P0.12	IO	Hall Sensor B-phase input/Timer3 channel 1/ADC channel 16/Comparator 0 positive input channel 2/P0.12
4	4	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	IO	Hall Sensor C-phase input/ADC channel 17/Comparator 0

087D	087E	Pin Name	Type	Description
				positive input channel 3/P0.13
5	5	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	IO	Comparator 0 Output/Motor PWM brake signal 1/SPI Clock/Timer0 channel 1/ADC Trigger 0/SIF/ADC channel 10/Comparator 0 positive input channel 4/P0.14
6		MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	IO	Motor PWM channel 0 high-side/UART0 TX(RX)/SPI Data Output/Timer0 channel 0/ADC Trigger1/Comparator 0 negative input/P0.15
	6	ADC_CH11/OPAx_OUT/LDO15/P2.7/ TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	IO	ADC channel 11/OPAx Output/LDO15 Output/P2.7/ADC Trigger1/Comparator 0 negative input/P0.15, built-in 10k pull-up resistor that can be enabled by software
7		ADC_CH11/OPAx_OUT/LDO15/P2.7	IO	ADC channel 11/OPAx Output/LDO15 Output/P2.7， built-in 10k pull-up resistor that can be enabled by software
	7	LDO5V	PWR	5V LDO output. A 1uF decoupling capacitor is required, and it should be as close as possible to the LDO5V pin.
8	8	VCC	PWR	Power suuply, input range 9~28V. If VCC is high than 20V, and the chip won't be set to sleep mode in application, a 1~2kΩ shunt resister is recommended to be placed between VCC and AVDD. Please refer to Chapter 21 for resister value. There must be a decoupling capacitor greater than or equal to 100uF between VCC pin and ground
9	9	HO1	O	A-phase PWM high-side output, controlled by P1.4's output signal. A 51Ω resister is required between HO1 Output and the Gate of MOS
10	10	LO1	O	A-phase PWM low-side Output, controlled by P1.5's output signal. Set GPIO1_F7654[7:4]=3, and GPIO3_POE[13]=1 A 51Ω resister is required between LO1 Output and the Gate of MOS
11	11	HO2	O	B-phase PWM high-side output, controlled by P1.5's output signal. A 51Ω resister is required between HO1 Output and the Gate of MOS
12	12	LO2	O	B-phase PWM low-side Output, controlled by P1.7's output signal. Set GPIO1_F7654[15:12]=3, and GPIO1_POE[12]=1 A 51Ω resister is required between LO2 Output and the Gate of MOS
13	13	HO3	O	C-phase PWM high-side output, controlled by P1.8's output signal. A 51Ω resister is required between HO1 Output and the Gate of MOS
14	14	LO3	O	C-phase PWM low-side Output, controlled by P1.9's output signal. Set GPIO1_FBA98[7:4]=3, and GPIO1_POE[15]=1 A 51Ω resister is required between LO3 Output and the Gate of MOS

087D	087E	Pin Name	Type	Description
15	15	AVSS	GND	System ground
16	16	OPA2_IP/P3.10	IO	OPA2 positive input /P3.10
17	17	OPA2_IN/P3.11	IO	OPA2 negative input/P3.11
18	18	OPA3_IN/P3.14	IO	OPA3 negative input/P3.14
19	19	OPA3_IP/P3.15	IO	OPA3 positive input /P3.15
20	20	UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/ CMP1_IP1/P2.4	IO	UART1 TX(RX)/Timer1 channel 0/ADC Trigger3/Comparator 1 positive input channel 1/P2.4，built-in 10k pull-up resistor that can be enabled by software
21	21	UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/ CMP1_IP2/P2.5	IO	UART1 TX(RX)/Timer1 channel 1/ADC Trigger0/Comparator 1 positive input channel 2/P2.5，built-in 10k pull-up resistor that can be enabled by software
22		SWCLK	I	SWD Clock, built-in fixed pull-up 10k resistor
	22	SWCLK/ TIM3_CH0/CMP1_IP3/P2.6	I	SWD Clock/ Timer3 channel 0/Comparator 1 positive input channel 3/P2.6, built-in fixed pull-up 10k resistor. SWCLK and P2.6 cannot be used simutaneously
23	23	SWDIO/P2.15/P0.0	IO	SWD Data/P2.15/P0.0, built-in fixed pull-up 10k resistor SWD Data IO/P2.15/P0.0 are bonded together at one singal chip pin. Please pay attention to the input/output enable of P2.15/P0.0, in case P2.15/P0.0 are output enabled right after POR which will cause swd communication failure. P2.15/P0.0 should NOT be both configurated as output.
24	24	RSTN/P0.2	IO	RSTN/P0.2, used as RSTN by default, a 10nF~100nF capacitor externally connected to the ground, and a 100k pull-up resistor inside. It is recommended to place a 10k-20k pull-up resistor between RSTN and AVDD on the PCB. If there is a pull-up resistor externally, the capacitance of RSTN is fixed to be 100nF.

Table 3-1 LKS32MC08x with Built-in 3P3N Driver Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P0.0												ADC_CH4, DAC_OUT
P0.1												ADC_CH6
P0.2												
P0.3						SCL		TIM2_CH0				ADC_CH7
P0.4						SDA		TIM2_CH1				ADC_CH8
P0.5												ADC_CH9
P0.6				UART1_TX(RX)			TIM1_CH0			CAN_RX		
P0.7				UART1_TX(RX)			TIM1_CH1			CAN_TX		
P0.8												
P0.9						SCL		TIM2_CH0				
P0.10						SDA		TIM2_CH1				
P0.11		HALL_IN0						TIM3_CH0				ADC_CH15/CMP0_IP1
P0.12		HALL_IN1						TIM3_CH1		CAN_RX		ADC_CH16/CMP0_IP2
P0.13		HALL_IN2								CAN_TX		ADC_CH17/CMP0_IP3
P0.14	CMP0_OUT		MCPWM_BKIN1		SPI_CLK		TIM0_CH1		ADC_TRIG0		SIF	ADC_CH10/CMP0_IP4
P0.15			MCPWM_CH0P	UART0_TX(RX)	SPI_DI(DO)		TIM0_CH0		ADC_TRIG1			CMP0_IN

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P1.0			MCPWM_CH0N	UART0_TX(RX)	SPI_DI(DO)							
P1.1					SPI_CS							
P1.2								TIM3_CH0				
P1.3								TIM3_CH1				ADC_CH5
P1.4	LRC		MCPWM_CH0P									
P1.5	HRC		MCPWM_CH0N									
P1.6			MCPWM_CH1P									
P1.7			MCPWM_CH1N									
P1.8			MCPWM_CH2P									
P1.9			MCPWM_CH2N									
P1.10			MCPWM_CH3P	UART0_TX(RX)		SCL	TIM0_CH0		ADC_TRIG2			ADC_CH13
P1.11			MCPWM_CH3N	UART0_TX(RX)		SDA	TIM0_CH1		ADC_TRIG3		SIF	
P1.12			MCPWM_CH1N									
P1.13					SPI_CLK		TIM0_CH0					
P1.14					SPI_DI(DO)		TIM0_CH1					
P1.15			MCPWM_CH2N									

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P2.0					SPI_CS			TIM2_CH1				
P2.1					SPI_CLK							ADC_CH14/ CMP1_IP0
P2.2												CMP1_IN
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS							REF
P2.4		HALL_IN0	MCPWM_CH2P	UART1_TX(RX)			TIM1_CH0		ADC_TRIG3	CAN_RX		CMP1_IP1
P2.5		HALL_IN1	MCPWM_CH2N	UART1_TX(RX)			TIM1_CH1		ADC_TRIG0	CAN_TX		CMP1_IP2
P2.6		HALL_IN2	MCPWM_CH3P					TIM3_CH0	ADC_TRIG1		SIF	CMP1_IP3
P2.7												ADC_CH11/ OPAx_OUT/ LDO15
P2.8				UART1_TX(RX)				TIM3_CH0				OSC_IN
P2.9					SPI_DI(DO)	SCL						ADC_CH12/ CMP0_IP0
P2.10					SPI_DI(DO)	SDA						
P2.11			MCPWM_CH1P					TIM2_CH0				
P2.12			MCPWM_CH1N					TIM2_CH1	ADC_TRIG2			
P2.13			MCPWM_CH3N					TIM3_CH1				
P2.14						SCL						
P2.15						SDA						

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P3.0												
P3.1												
P3.2												
P3.3												
P3.4												
P3.5												
P3.6												
P3.7												
P3.8												
P3.9				UART1_TX(RX)				TIM3_CH1				OSC_OUT
P3.10												OPA2_IP
P3.11												OPA2_IN
P3.12												
P3.13	HRC		MCPWM_CH0N									
P3.14												OPA3_IN
P3.15												OPA3_IP

4 Package Size

4.1 LKS32MC087DM6S8(B)/ LKS32MC087EM6S8(B)

SSOP24L:

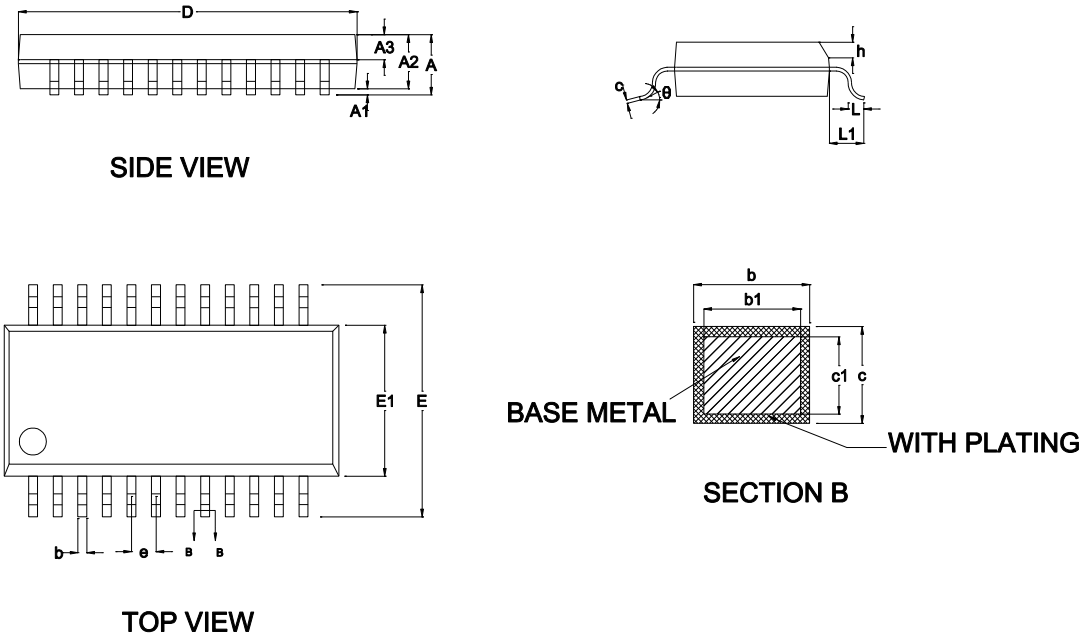

Fig. 4-1 LKS32MC087DM6S8(B)/ LKS32MC087EM6S8(B) Package Diagram

Table 4-1 LKS32MC087DM6S8(B)/ LKS32MC087EM6S8(B) Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

5 Electrical Characteristics

Table 5-1 LKS32MC08x with Built-in 3P3N Driver Electrical Absolute Characteristics

Parameter	Min	Max.	Unit	Description
MCU Power supply voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Power supply voltage (VCC)	-0.3	+40.0	V	
5V LDO output current		40	mA	
Operating Temperature	-40	+105	˚C	
Storage temperature	-40	+150	˚C	
Junction temperature	-	150	°C	
Pin temperature (soldering for 10 seconds)	-	260	°C	

Table 5-2 LKS32MC08x with built-in 3P3N driver Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Power supply voltage (AVDD)	3.0	5	5.5	V	The AVDD reset level of version A chip is 2.2V ± 0.2V
	2.2				The AVDD reset level of version B chip is 2.7V ± 0.2V
Analog power voltage ($AVDD_A$)	3.3	5	5.5	V	ADC use 2.4V internal reference
	2.8	5	5.5	V	ADC use 1.2V internal reference
Gate Driver Power supply voltage (VCC)	7.5		28	V	When VCC＜7.5V, 3P3N Gate driver will be shut down while MCU could still work normally

OPA could work under 2.2V, but the output range will be limited.

Table 5-3 LKS32MC08x with Built-in 3P3N Driver Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Power Supply Voltage (AVDD)	2.2	5	5.5	V	
Analog Supply Voltage($AVDD_A$)	2.8	5	5.5	V	

OPA could work under 2.2V, but the output range will be limited.

Table 5-4 LKS32MC08x with Built-in 3P3N Driver ESD parameters

Item	Min.	Max.	Unit
ESD test (HBM)	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-5 LKS32MC08x with Built-in 3P3N Driver Latch-up parameters

Item	Min.	Max.	Unit

Latch-up current (85℃)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

Table 5-6 LKS32MC08x with Built-in 3P3N Driver IO Absolute Characteristics

Parameter	Description	Min	Max.	Unit
V_{IN}	GPIO signal input voltage range	-0.3	6.0	V
HO_x	HO_x (x=1~3) input voltage range	VCC-15	VCC	V
LO_x	LO_x(x=1~3) input voltage range	-0.3	15	V
I_{INJ_PAD}	Maximum Injection Current of a Single GPIO	-11.2	11.2	mA
I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 5-7 LKS32MC08x with Built-in 3P3N Driver IO DC Parameters

Parameter	Description		AVDD	Conditions	Min.		Max.	Unit
V_{IH}	High input level of digital IO		5V	-	0.7*AVDD			V
			3.3V		2.0			
V_{IL}	Low input level of digital IO		5V	-			0.3*AVDD	V
			3.3V				0.8	
V_{HYS}	Schmidt hysteresis range		5V	-	0.1*AVDD			V
			3.3V					
I_{IH}	Digital IO current consumption when input is high		5V	-			1	uA
			3.3V					
I_{IL}	Digital IO current consumption when input is low		5V	-	-1			uA
			3.3V					
V_{OH}	High output level of digital IO			Current = 11.2mA	AVDD-0.8			V
V_{OL}	Low output level of digital IO			Current = 11.2mA			0.5	V
R_{pup}	Pull-up resistor*	Reset pin			100	200	400	kΩ
		Normal pin			8	10	12	
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit				100		200	Ω
C_{IN}	Digital IO Input-capacitance		5V	-			10	pF
			3.3V					

*Only some IOs have built-in pull-up resistors, see section “Pin Function Description” for details.

Table 5-1 LKS32MC08x Module Current/IDD

模块	Min	Typ	Max	单位
Comparator x1		0.005		mA
OPA x1		0.450		mA
ADC		3.710		mA
DAC		0.710		mA
Temp Sensor		0.150		mA
Band-Gap		0.154		mA
4MHz RC Clock		0.105		mA
PLL		0.080		mA
CPU+flash+SRAM (96MHz)		8.667		mA
CPU+flash+SRAM (12MHz)		1.600		mA
CRC		0.070		mA
DSP		3.421		mA
UART		0.107		mA
DMA		1.340		mA
MCPWM		0.053		mA
TIMER		0.269		mA
SPI		0.500		mA
IIC		0.500		mA
CAN		2.200		mA
Sleep Mode	10	30	50	uA

All the test results above are based on the chips running 96MHz at room temperature with 5V as power supply. Device charactoristics may vary due to process accuracy.

6 Analog Characteristics

Table 6-1 LKS32MC08x with Built-in 3P3N Driver Analog Characteristics

Parameter	Min.	Normal	Max.	Unit	Description
Analog-to-Digital Converter (ADC)					
Power Supply	2.8	5	5.5	V	ADC use 2.4V internal reference
	3.3	5	5.5	V	ADC use 1.2V internal reference
Sampling rate		3		MHz	$f_{adc}/16$
Differential input signal range	-2.352		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-3.528		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
Single-ended input signal range	-0.3		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-0.3		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
	-0.3		AVDD*0.9	V	REF2VDD=1, Gain=1; REF=AVDD
	-0.3		AVDD+0.3	V	REF2VDD=1, Gain=2/3 , REF=AVDD, limited by IO diode clamp
The differential signal is usually the signal output from the OPA inside the chip to the ADC; The single-ended signal is usually the sampled signal from the external input through IO. Whether using an internal/external reference, the signal amplitude should not exceed ±98% of the ADC signal range. In particular, when using an external reference, it is recommended that the sampled signal not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	100k			Ohm	
Input Capacitance		10pF		F	
Reference Voltage (REF)					
Power Supply	2.2	5	5.5	V	
Output Deviation	-9		9	mV	
Rejection Ratio of Power Supply		70		dB	
Temperature Coefficient		20		ppm /°C	
Output Voltage		1.2		V	
Digital-to-Analog Converter (DAC)					
Power Supply	2.2	5	5.5	V	

Parameter	Min.	Normal	Max.	Unit	Description
Load Resistance	5k			Ohm	Output BUFFER is on
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational Amplifier (OPA)					
Power Supply	2.8	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load Resistance	20k			Ohm	
Load Capacitance			5p	F	
Input Common Mode Voltage Range (VICM)	0		AVDD	V	
Output Signal Range	0		2*Vcm	V	Under minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differen- tial input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification xOFFSET
Common Mode Voltage (Vcm)	1.65	1.9	2.2	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".
Common Mode Rejection Ratio (CMRR)		80		dB	
Power Supply Rejection Ratio (PSRR)		80		dB	

Parameter	Min.	Normal	Max.	Unit	Description
Load Current			500	uA	
Slew Rate		5		V/us	
Phase Margin (PM)		60		De-gree	
Comparator (CMP)					
Power Supply	2.2	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET		5	10	mV	
Delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'

Description of Analog Register Table:

Address space of 0x40000040 to 0x40000050 are the calibration registers of each analog module. These registers will be set to a unique calibration value in factory. Generally, users are advised not to configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x40000020 to 0x4000003c are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers will be configured according to the actual application scenarios.

7 Power Management System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

The chip is powered by a 7.5V ~ 28V single supply to save the power supply costs outside the chip. An internal LDO5 supply the power of MCU. And all internal digital circuits and PLL modules in the MCU are powered by an internal LDO15.

The LDO15 automatically turns on after power-on, without software configuration, and the LDO output voltage can be adjusted through software.

LDO15 has been calibrated before it leaves the factory.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.1V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation

8 Clock System

The clock system consists of a 32KHz RC oscillator, an internal 4MHz RC oscillator and a PLL.

The 32k RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode. The 4MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz.

Both 32k and 4M RC clocks will been through factory calibration. In the range of -40 ~ 105 ℃, the accuracy of the 32K RC clock is ± 50%, and the accuracy of the 4M RC clock is ± 1%

The 4M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 4M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 4M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be also turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and enabled by software.

9 Bandgap Voltage Reference

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = ’0’. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

The voltage reference can be measured by setting REF_AD_EN = ’1’ and via IO P2.3.

10 ADC module

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 4M RC clock and PLL should be turned on first, and the operating frequency of ADC should be selected. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

f_{adc} ADC takes 16 ADC clock cycles to complete one conversion, of which 12 are conversion cycles and 4 are sampling cycles. i.e. = f_{conv} /16. When the ADC clock is set to 48MHz, the conversion rate is 3Msps. The sampling cycle can be set by configuring the SAMP_TIME register in SYS_AFE_REG7. It is required to be set to more than 6 (including 6), i.e., the sampling time of 10 ADC clk or more.
The recommended value is 8, which corresponds to the ADC output data rate of 2MHz.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, one-time 1 to 20 channels scanning mode, continuous 1 to 20 channels scanning mode. It has a set of 20 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

The ADC has two gain modes, which are set by GAIN_SHAx, corresponding to 1x and 2/3 x gain setting. 1x gain corresponds to an input signal range of ± 2.4V, and 2/3 gain corresponds to an input signal range of ± 3.6V. When measuring the output signal of the OPA, select the specific ADC gain according to the maximum signal that the OPA may output.

11 Operational Amplifier

2-channel of rail-to-rail OPAs are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 2-channels amplifiers by setting OPAOUT_EN <1:0>, and send it to the P2.7 IO port through a buffer for measurement. Because of the BUFFER, the operational amplifier is also able to send one output signal in the normal working mode.

When the chip is powered on, the amplifier module is OFF by default. It can be turned on by setting OPAxPDN = '1', and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes that are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 2-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay can be set to 0.15 us, and can be set to be less than 30 ns. The hysteresis voltage can be set to 20mV/0mV by CMP_HYS.

The signal sources of the positive and negative inputs can be programmed by register CMP_SELP<2:0> and CMP_SELN<1:0>. For details, please refer to the analog register description.

When the chip is powered on, the comparator module is OFF. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

13 Temperature Sensor

The chip has a temperature sensor with an accuracy of ±2°C in -40~85℃ and ±3°C in -40~105℃ typically. The operating temperature of chips will be corrected before leaving the factory, and the corrected value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1', and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 DAC

The chip has a 1-channel 12 bit DAC, and the maximum range of the output signal can be set to 1.2V/4.8V through the register DAC_GAIN<1:0>.

The 12bit DAC can be output via IO port P0.0 by setting register DACOUT_EN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output code rate of the DAC is 1MHz.

When the chip is powered on, the DAC module is OFF. DAC can be turned on by setting DAC12BPDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor

- 32-bit Cortex-M0 + DSP dual-core processor
- 2-wire SWD debug pin
- System frequency is up to 96MHz

16 Storage

16.1 Flash

- Built-in flash including 32kB/64kB main storage area and 1kB NVR
- Available for repeated erasure and writing for at least 20,000 times
- Data retention at room temperature 25℃ for up to 10 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size is 512 bytes. The data can be erased and written according to Sector. It supports runtime programming. While one Sector is erased and written, another Sector can be read and accessed at the same time.
- Flash data anti-theft (any value other than 0xFFFFFFFF must be written to the last word)

16.2 SRAM

- Built-in 8kB SRAM

17 Motor Control PWM

- MCPWM operating frequency is up to 96MHz
- Supports up to 3 pairs of complementary PWM output with adjustable phase
- The width of dead-zone in each channel can be configured independently
- Support edge-aligned PWM mode
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simultaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support 4-channel capture mode for measuring external signal/pulse width
- Support 4-channel comparison mode for timed interruption of edge-aligned PWM

19 Hall Sensor Interface

- Built-in 1024 cycles filtering at most
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 General Peripherals

- One UART, full-duplex operation, support 7/8 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, with write protection and 2/4/8/64 seconds reset interval.

21 3-phase P/N MOS Gate Drive Module

21.1 Module parameter

Table 21-1 LKS32MC08x with Built-in 3P3N Driver Driver Module Parameters

Symbol	Parameter	Condition	Min	Typical	Max.	unit
Static parameters						
VCC_ON	VCC undervoltage recovery voltage		5.8	6.5	7.4	V
VCC_UVLO	VCC undervoltage threshold voltage		5.4	6	6.8	V
VCC_HYS	Undervoltage hysteresis		0.3	0.5	0.8	V
IQC	Static power supply	VIN=0V	0.3	0.5	1.0	mA
VDD	5V LDO output voltage		4.7	5.0	5.3	V
VIH	Logic '1' flip voltage		2.2			V
VIL	Logic '0' turnover voltage				0.6	V
I_SOURCE	Input signal logic '1' bias current	VIN=5V		32	100	uA
I_SINK	Input signal logic '0' bias current	VIN=0V			1	uA
VHO	HOx(x=1~3) output turn-on voltage (because HO drives PMOS, low level corresponds to the turn-on)		VCC-11	VCC-9.5	VCC-8	V
V_{LO}	LOx(x=1~3) output turn-on voltage		8.5	10	11.5	V
I_{HO+}	HOx(x=1~3) input sink current	HOx=VCC	-	35	-	mA
I_{HO-}	HOx(x=1~3) output source current	HOx=VCC-10V	-	300	-	mA
I_{LO+}	LOx(x=1~3) output source current	LOx=0V	-	60	-	mA
I_{LO-}	LOx(x=1~3) input sink current	LOx=10V	-	300	-	mA
T_{SD}	TSD temperature		-	150	-	℃
$T_{RECOVER}$	TSD recovery temperature		-	135	-	℃
I_{Ldo}	Power supply capacity			40		mA
Dynamic parameters (CL=1nF)						
T_{ON}	Turn-on delay		-	80	-	ns

T_{OFF}	Turn-off delay		-	30	-	
TH_R	HOx rise time		-	50	-	
TH_F	HOx falling time		-	400	-	
TL_R	LOx rise time		-	200	-	
TH_F	LOx falling time		-	50	-	
DT	Built-in dead-zone time		-	100	-	

The input and output waveforms of the P/N MOS drive module are as shown below. As shown in the figure, HIN/LIN is the output signal of the MCPWM module inside the chip. For HIN, the output high level corresponds to the HO output low level, thereby driving the high-drive PMOS to turn on. For LIN, the output high level corresponds to the LO output high level, thereby driving the low-drive NMOS to turn on. Therefore, the polarity selection of P and N in MCPWM register MCPWM_IO01/MCPWM_IO23 does not need to be reversed.

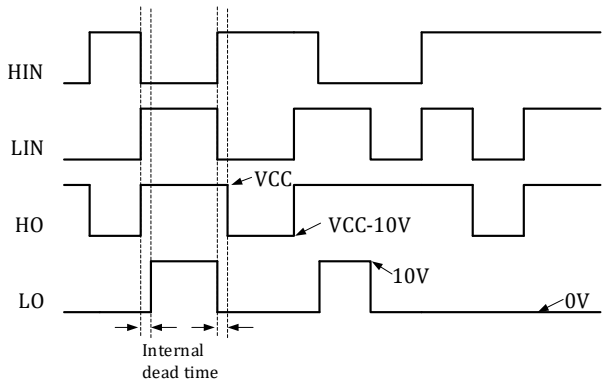

Fig. 21-1 Drive Module Input and Output Timing Sequence Waveform

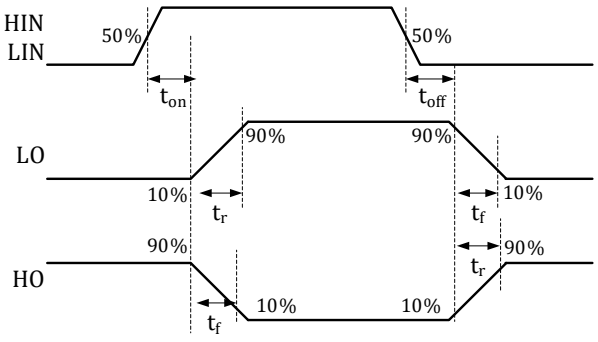

Fig. 21-2 Drive Module Output Change Edge Timing Waveform

21.2 Recommended Application Diagram

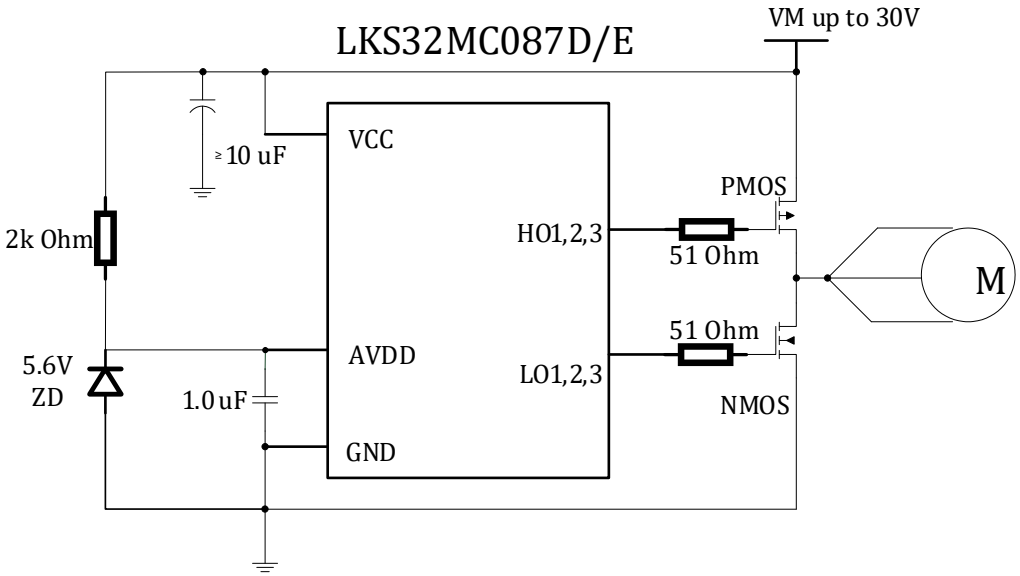

Fig. 21-3 LKS32MC087DM6S8(B)/LKS32MC087EM6S8(B) Typical Drive Module Application Diagram

The output pin signal LO1/HO1 of the drive module corresponds to the MCPWM function output of corresponding GPIO P1.4/P1.7, LO2/HO2 corresponds to the MCPWM function output of corresponding GPIO P1.5/P1.8, and LO3/HO3 corresponds to the MCPWM function output of the corresponding GPIO P1.6/P1.9. However, the address to be configured is MCPWM_SWAP=1 of 0x4001_1C7C. See the user manual for details.

A 51Ω resistor is recommended between HO1/HO2/HO3/LO1/LO2/LO3 output pin and the gate of the P/NMOS when phase current is larger than 2A.

In applications where VCC is higher than 20V, the AVDD pin is powered by the chip's own LDO5V pin, and the chip does not need to sleep, it is recommended to add a 1k~2k ohm shunt resistor between VCC and AVDD. This resistor is connected between the input and output terminals of internal 5V LDO to share the partial heat dissipation function. The resistor needs to be placed at a distance from the chip (for 055D and 057E, if the AVDD pin is powered by an external 5V power supply, this resistor is not required).

The calculation of resistance value must be based on the following formula:

R>=(VCC-AVDD)/I

Whereof, I is the total power consumption on the 5V power supply, including the power consumption of the MCU and the power consumption of 5V peripheral device (e.g., HALL).

In case an external shunt resistor is connected, a 5.6V voltage regulator tube should be mounted on the AVDD pin.

Meanwhile, in applications where a resistor is connected between VCC and AVDD, please note that the RC constant on RSTN should not be too large. It is recommended to keep the RC constant to be 1ms. I.e., in case the external resistance of the chip is not added to 5V, when the internal pull-up

resistance is 100k, the capacitance on RSTN is selected as 10nF. If a 10k or 20k pull-up resistor is added externally, the capacitance on RSTN is selected as 100nF.

There must be a decoupling capacitor ≥100uF between VCC pin and ground.

The gate driver signal polarity is as follow:

Table 21-1 LKS32MC087DM6S8(B)/LKS32MC087EM6S8(B) gate driver polarity truth table

{HIN,LIN}	HO	LO	
00	1	0	All off
01	1	1	Low side open
10	0	0	High side open
11	1	0	All open, will trigger hardware protection

22 Special IO Multiplexing

Notes for Special IO Multiplexing of LKS08x

The SWD protocol includes two signals: SWCLK and SWDIO. SWCLK is a clock signal. To the chip, it is an input and will always be an input. SWDIO is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Users could use two IOs of SWD as GPIOs P0.0/P2.15. The precautions are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.
- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In SSOP24 package and QFN40 package, SWDIO is directly bonded with P0.0 and P2.15, and the corresponding GPIO can be directly enabled. It is recommended that SWDCLK keep unchanged (constant 1 or constant 0) when multiplexing SWDIO

For LKS087E, SWDCLK is bonded with P2.6 and the corresponding GPIO can be directly enabled. If SWDIO and SWDCLK are multiplexed at the same time, considerations for SWDCLK multiplexing are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to

ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.

- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

When SWDCLK and SWDIO pins are used as GPIO, they should not act at the same time. That is, when SWDCLK multiplexing is enabled and changes, SWDIO can remain at level 0 (similar to time division multiplexing).

For RSTN signal, the default is for the external reset pin of LKS08x chip.

LKS08x allow users to multiplex RSTN as other IOs, and the multiplexed IO is P0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

23 Ordering Information

The package type is divided into Tray package and Reel package. The number of chips in the specific package is determined by the package form and package type, and is no longer distinguished by the chip model.

Tray packaging information is shown in the table below

Packaging form	Quantity per plate /tube	Number of inner boxes	Number of outer boxes
SOP16/ESOP16L	3000/plate	6000PCS	48000PCS
SSOP24	4000/plate	8000PCS	64000PCS
SS0P24	50/tube	10000PCS	4000/100000PCS
QFN 8*8	260/plate	2600PCS	15600PCS
QFN 4*4/5*5/6*6	490/plate	4900PCS	29400PCS
QFN 3*3	5000/plate	5000PCS	40000PCS
LQFP48/TQFP48 0707	250/plate	2500PCS	15000PCS
LQFP64 1010	160/plate	1600PCS	9600PCS
LQFP100 1414	90/plate	900PCS	5400PCS
TSSOP20/28	4000/plate	8000PCS	64000PCS

Reel packaging information is shown in the table below

Packing category		Quantity per plate /tube	Quantity per box	Number of box-es per carton	Number of outer boxes
Braid-13 inch	SOP/ESOP8	4000	8000	8	64000
Braid-13 inch	SOP/ESOP16	3000	6000	8	48000
Braid-13 inch	SSOP24	4000	8000	8	64000
Braid-13 inch	TSSOP20	4000	8000	8	64000
Braid-13 inch	D/QFN3*3	5000	10000	8	80000
Braid-13 inch	D/QFN4*4	5000	10000	8	80000
Braid-13 inch	D/QFN5*5	5000	10000	8	80000
Tube installation	SOP16	50	10000	10	100000
Tube installation	SOP14/SSOP24	50	10000	10	100000
Tube installation	TSSOP24	54	6480	6	38880

24 Version History

Table 24-1 Document Version History

Date	Version No.	Instruction
2024.12.12	1.83	Description of Added ADC Saturation Range
2024.08.06	1.82	Order package information update to confirm package information by package type and package form
2024.01.26	1.81	Modified 2 Device Selection Guide
2023.12.12	1.8	Added description of pull-up resistance values
2023.11.09	1.7	OPA OFFSET Adds the description, Renewal storage temperature
2023.06.04	1.6	Modify pin multiplex function of P3.13、P1.12 and P1.15
2023.04.28	1.59	Add B-version chip with AVDD power supply range of 3.0-5.5V Modify Package Name
2023.04.03	1.58	Adjust AVDD range from 2.2~5.5 to 3.0~5.5V
2023.03.18	1.57	Modified the description of clock accuracy
2023.02.11	1.56	Revise current of P/N MOS Gate Drive Module
2023.01.13	1.55	Add ordering information
2022.11.15	1.54	Revise special IO Multiplexing
2022.11.07	1.53	Add connection resistance between IO and internal analog circuit
2022.10.28	1.52	Add characteristic of common mode voltage
2022.10.20	1.51	Revise VCC pin description
2021.04.13	1.5	The whole family device selection guide
2020.11.30	1.4	Revise the pin function description of 087E
2020.11.3	1.3	Revise the driver module parameters
2020.09.16	1.2	Revise partial parameter function description
2020.08.28	1.1	OPA1 input pin polarity adjustment
2020.04.20	1.0	Initial version

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For earlier versions, please refer to this document.