Linko Semiconductor Co., Ltd.

LKS32MC05x with built-in 3P3N driver Datasheet

1 Overview

1.1 Function

LKS32MC055DL6S8/LKS32MC055EL6S8/LKS32MC057EM6S8/ LKS32MC057FM6S8 are 32-bit MCU targeting motor control applications. With all modules required for common motor control systems and three-phase P/N MOS gate driver, it can directly drive three-channel P/N MOS power device.

- **Features**
  - 96MHz 32-bit Cortex-M0 core
  - Low power sleep mode
  - Integrated three-phase P/N MOS gate driver
  - Industrial temperature range
  - High ESD and group pulse reliability

- **Memory**
  - 32kB Flash with optional encryption and 128-bit chip unique identifier
  - 2.5K RAM
- **Operating Conditions**
  - 7.5~32V (Maximum: 40V), single power supply, with an integrated internal 5V LDO for partial power supply for internal MCU of chip
  - Operating Temperature: -40~105℃
- **Clock**
  - 4MHz built-in high-precision RC clock, with an accuracy of ± 1% at -40 ~ 105 ℃
  - 64KHz built-in low-speed clock for low-power mode
  - Internal PLL up to 96 MHz clock
- **Peripheral Modules**
  - Two UARTs
  - One SPI, support master-slave mode
  - One IIC, support master-slave mode
  - Two 16-bit timers, support capture and edge-aligned PWM function
  - Two 32-bit timers, support capture and edge-aligned PWM function;
  - Motor control PWM module, supports 8 channels of PWM output, independent dead-band control
  - Hall signal interface with speed measurement and debouncing function
  - Hardware watchdog

- **Analog Modules**
  - Integrated one 12-bit SAR ADC, 2Msps sampling and conversion rate, 16 channels in total
  - Integrated 2 operational amplifiers, differential PGA mode available
  - Integrated two comparators
  - Integrated 12-bit DAC digital-to-analog converter
  - ± 2 ℃ built-in temperature sensor
  - Built-in 1.2V 0.8% precision voltage reference source
  - Built-in one low-power LDO and power monitoring circuit
  - Integrated RC clock with high precision and low temperature drift

- **Packaging:**

Table 1-1 Packaging summary Table for LKS32MC05x with Built-in 3P3N Driver

Device	Package
LKS32MC055DL6S8	SOP16
LKS32MC055EL6S8	ESOP16
LKS32MC057EM6S8	SSOP24L
LKS32MC057FM6S8	SSOP24L

1.2 Main Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 2 channels high-speed OPAs and 2 channels comparators, meeting the different needs of single resistance/double resistance current sampling topology structure;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be directly input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed high current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Single power 7.5~32V supply, integrated 5V LDO internally;
- The three-phase P/N MOS gate driver is integrated;
- Support IEC/UL60730 functional security certification

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors;

1.3 Naming Conventions

LKS32 MC 051 D 2 M 6 S 8 B (XX)

Device series

LKS32	= 32bit MCU
LKS5	= Gate Driver Products
LKS6	= Power IC Product

Product type

MC	= Motor Control Applications
AT	= Automobile Applications
RV	= RISC-V for Motor Control

Device sub family

051/052/057	= 2.2~5.5V, 1 ADC, 2 PGA
051D/054D	= 2.2~5.5V, 1 ADC, 2 PGA, 6N driver
054DO	= 2.2~5.5V, 1 ADC, 2 PGA, 6N Driver, 5V LDO
055D/055E/ 057E/057F	= 7.5~28V, 1 ADC, 2 PGA, 3P3N Driver

Gate Driver Functions

D	= 3P3N Gate Driver
E/DL	= 3P3N + 5V LDO
S/F	= 6N Gate Driver
SL/FL	= 6N + 5V LDO
K	= High V 6N Gate Driver
O/L5	= 5V LDO/DCDC
L3	= 3.3V/3V LDO
N	= DCDC
P	= 3P3N/4P4N DrMOS
Q	= 6N/8N DrMOS
PL3	= 3P3N DrMOS + 3.3VLDO
PL5	= 3P3N DrMOS + 5VLDO
QL	= 6N DrMOS + LDO
X	= PHY
XL	= PHY + LDO

PKG/Driver Ver

2	= 2nd Ver
S	= S 侧面上锡

Pin count

L	=16 pins
H	= 20 pins
M	= 24 pins
Y	=28 pins
K	= 32 pins
F	= 40 pins
G	= 42 pins
U	= 44 pins
C	= 48 pins
N	= 52 pins
S	= 54pins
E	= 60 pins
R	= 64 pins
P	= 80 pins
V	=100 pins
Q	=128 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory
D	=384Kbyte Flash Memory
E	=512Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

MCU Ver

B	= B ver

Options

TR	= Tape and reel packing
P	= ES

Fig. 1-1 Naming Conventions of LKS32MC057EM6S8 Components

1.4 System Resource

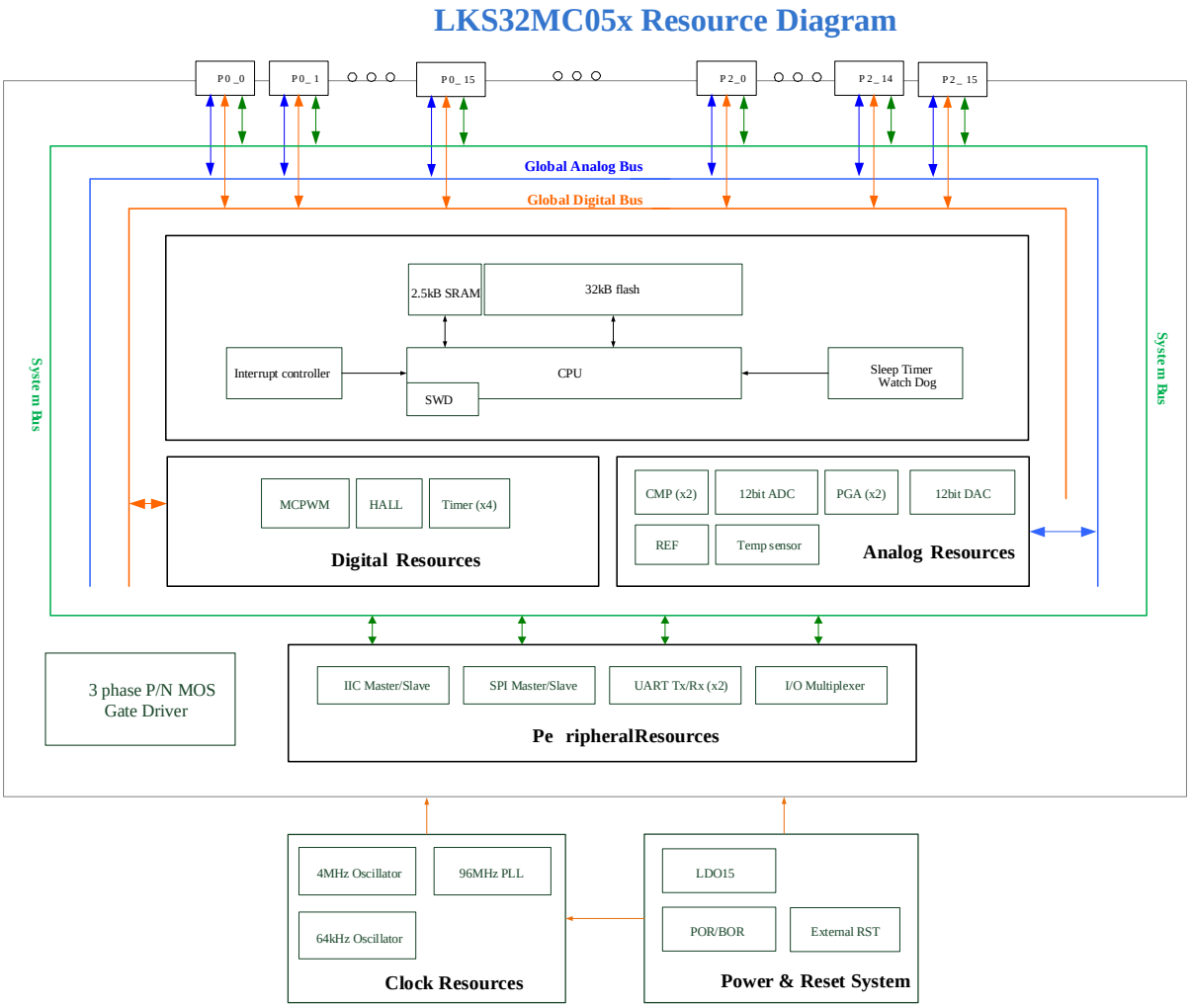

Fig. 1-2 System Block Diagram of LKS32MC05x with Built-in 3P3N Driver

1.5 FOC System Example

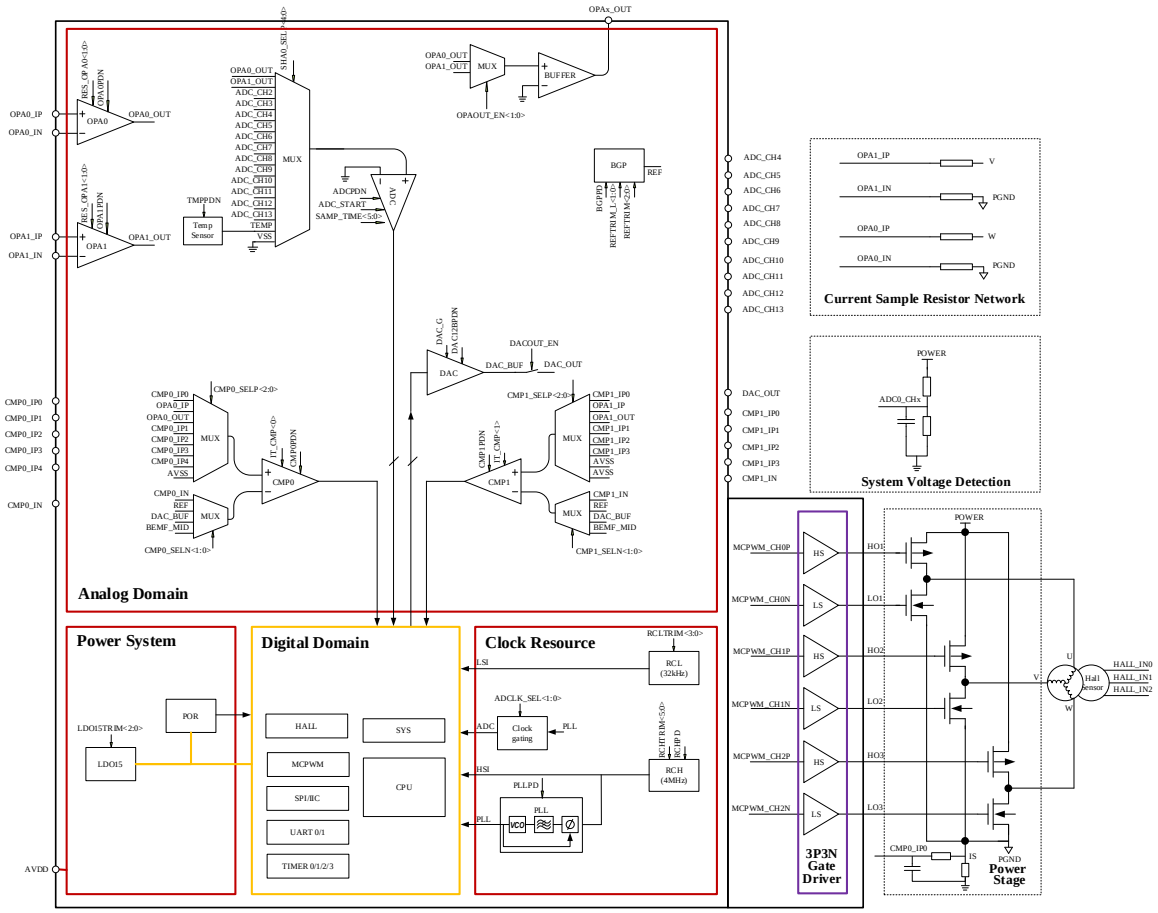

Fig. 1-3 LKS32MC05x with Built-in 3P3N Driver Simplified Schematic of FOC System

2 Device Selection Guide

Table 2-1 LKS05x family device selection guide

	Freq. (MHz)	Flash (kB)	RAM (kB)	ADC Ch.	DAC	CMP	CMP Ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver Current (A)	Gate Driver Power (V)	Floating G (V)	Others	Package
LKS32MC051C6T8	96	32	2.5	12	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes							TQFP48
LKS32MC051DC6T8	96	32	2.5	11	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20	200		TQFP48
LKS32MC052K6Q8	96	32	2.5	8	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes							QFN5*5 32L-0.75
LKS32MC054DF6Q8	96	32	2.5	9	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20	200		QFN5*5 40L-0.75
LKS32MC054DOF6Q8	96	32	2.5	9	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC055DL6S8	96	32	2.5	3	12BITx1	2	4	1	1 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~32		5V LDO	SOP16L
LKS32MC055EL6S8	96	32	2.5	4	12BITx1	2	6	1	3 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~32		5V LDO	SOP16L
LKS32MC057M6S8	96	32	2.5	6	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes							SSOP24L
LKS32MC057EM6S8	96	32	2.5	6	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~32		5V LDO	SSOP24L
LKS32MC057FM6S8	96	32	2.5	6	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~32		5V LDO	SSOP24L

3 Pin Assignment

3.1 Pin Assignment

3.1.1 Special Notes

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.
SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32MC057EM6S8

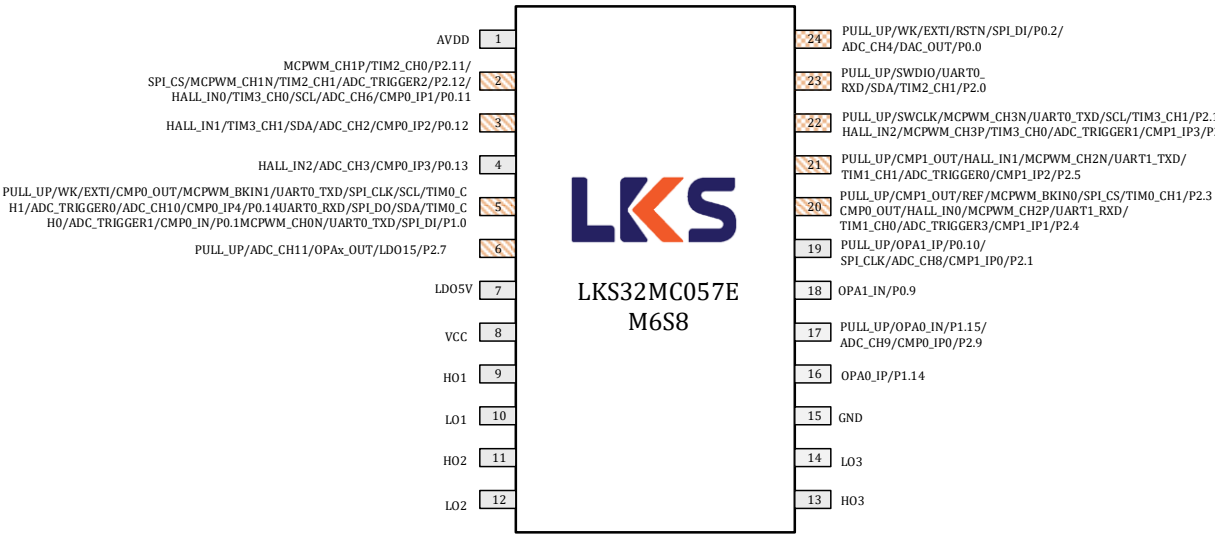

Fig. 3-1 LKS32MC057EM6S8 Pin Assignment

3.1.3 LKS32MC057FM6S8

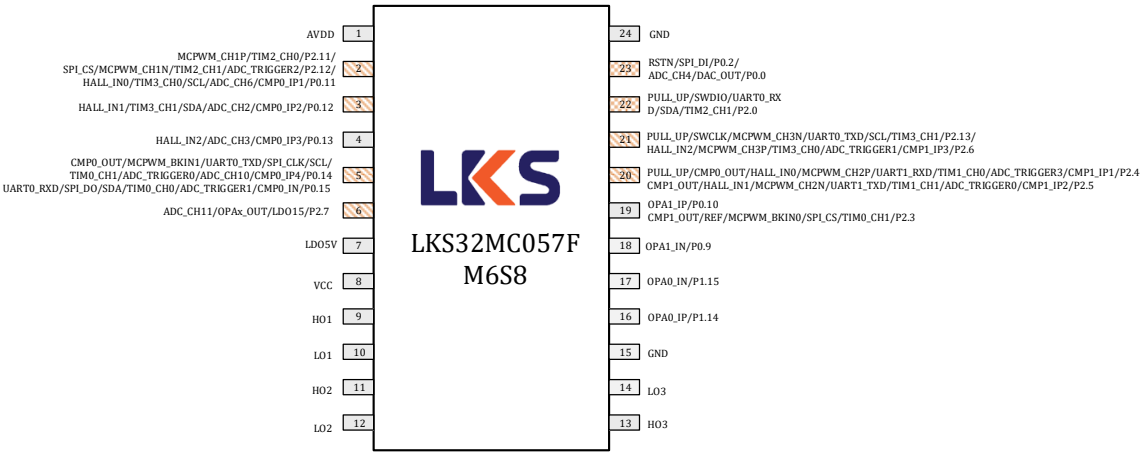

Fig. 3-2 LKS32MC057FM6S8 Pin Assignment

3.1.4 LKS32MC055DL6S8

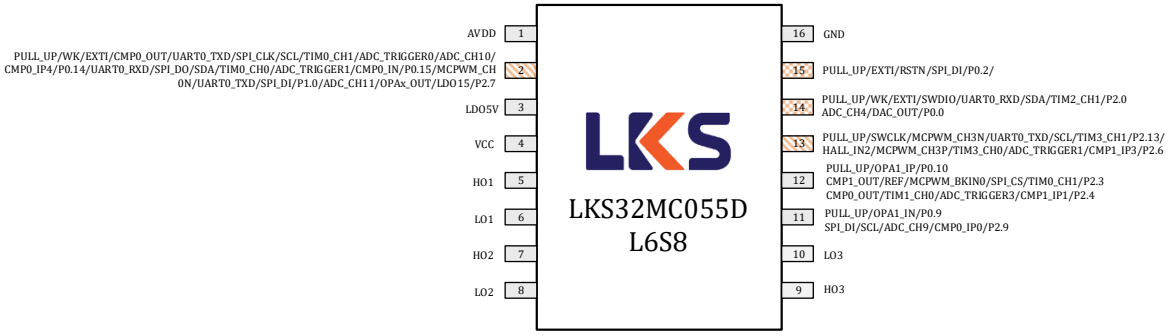

Fig. 3-3 LKS32MC055DL6S8 Pin Assignment

3.1.5 LKS32MC055EL6S8

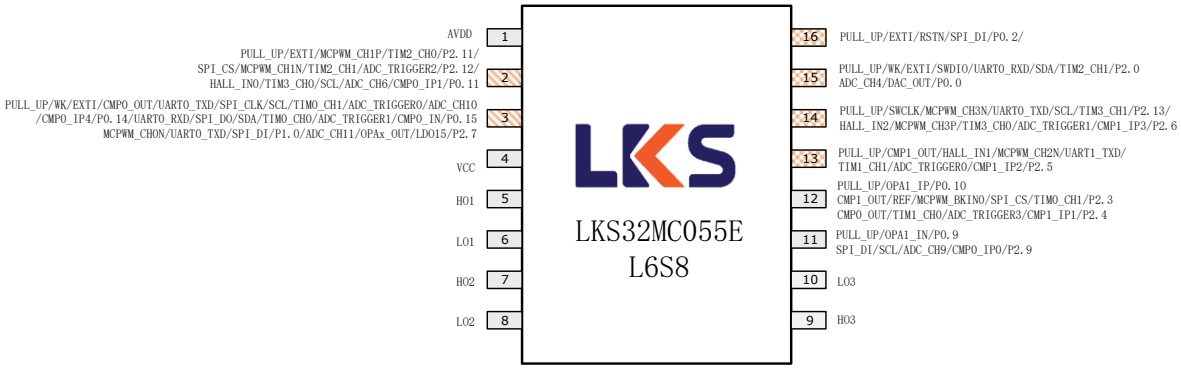

Fig. 3-4 LKS32MC055EL6S8 Pin Assignment

3.1.6 Inner Driver Connection Diagram

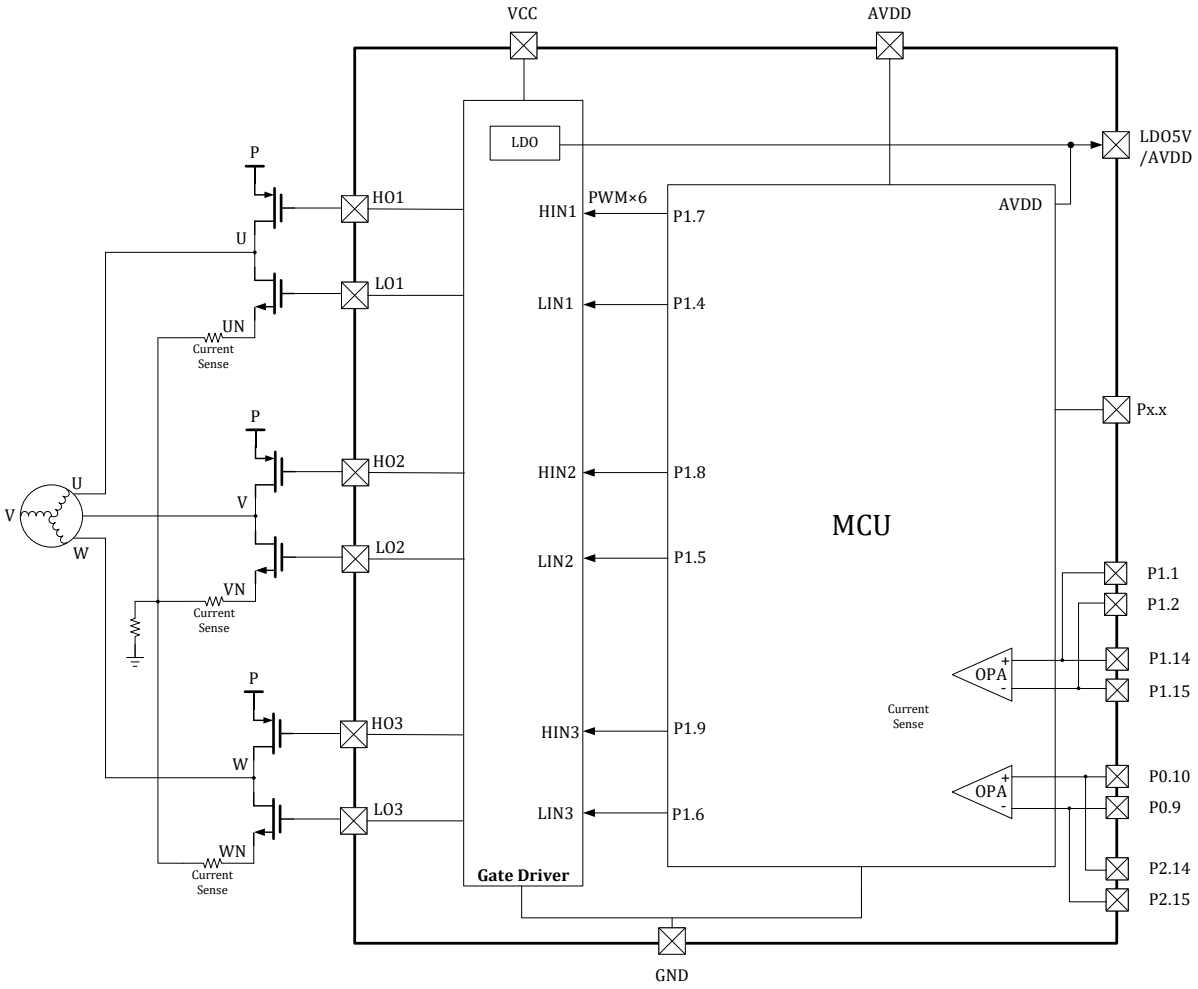

Fig. 3-5 Schematic diagram of inner driver connection

Notice: Do not pull up the LDO before the VCC is powered on. Otherwise, the LDO may fail to start after the VCC is powered on.

3.2 Pin Function Description

Table 3-1 LKS32MC05x with Built-in 3P3N Driver Pin Function Description

Chip pin No.				Name	Software number	Functions
055D	055E	057F	057E			
	0			GND	GND	Ground Pin, pin 0 is the bottom pad of the 055E package.
1	1	1	1	AVDD	PWR	For the 055D, 057E and 057F product, AVDD is the low-voltage power supply with a power supply range of 2.2~5.5V. In applications with good heat dissipation conditions, it can be directly connected to the LDO5V pin of the chip. To reduce the system power consumption and use the 5V power supply generated by an external DC or charge pump, connect this pin to the external 5V power supply For the 055E product, AVDD is the output pin of chip 5V LDO and the chip shall be connected with a 1uF decoupling capacitor, and it should be as close as possible to the LDO5V pin.
	2	2	2	MCPWM_CH1P/TIM2_CH0/P2.11	IO	Motor PWM channel 1 high side/Timer2 channel 0/P2.11

	2	2	2	SPI_CS/MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	IO	SPI CS signal/motor PWM channel 1 low side/Timer2 channel 1/ADC trigger signal 2/P2.12
	2	2	2	PULL_UP/EXTI/HALL_IN0/SCL/TIM3_CH0/ADC_CH6/CMP0_IP1/P0.11	IO	Pull up/External interruption/Hall sensor phase A input/IIC clock/Timer3 channel 0/ADC channel 6/comparator 0 positive terminal input channel 1/P0.11, built-in 10k pull-up resistor that can be enabled by software
		3	3	PULL_UP/EXTI/HALL_IN1/SDA/TIM3_CH1/ADC_CH2/CMP0_IP2/P0.12	IO	Pull up/External interruption/Hall sensor B phase input/IIC data/Timer3 channel 1/ADC channel 2/Comparator 0 positive terminal input channel 2/P0.12, built-in 10k pull-up resistor that can be enabled by software
		4	4	EXTI/HALL_IN2/ADC_CH3/CMP0_IP3/P0.13	IO	External interruption/Hall sensor C phase input/ADC channel 3/Comparator 0 positive input channel 3/P0.13
2	3	5	5	PULL_UP/EXTI/CMP0_OUT/MCPWM_BKIN1/UART0_TX(RX)/SPI_CLK/SCL/TIM0_CH1/ADC_TRIG0/ADC_CH10/CMP0_IP4/P0.14	IO	Pull up/External interruption/Comparator 0 output/motor PWM termination signal 1/UART0 TX(RX)/SPI clock/IIC clock/Timer0 channel 1/ADC trigger signal 0/ ADC channel 10/Comparator 0 positive terminal input channel 4/P0.14, built-in 10k resistor that can be enabled by software
2	3	5	5	PULL_UP/EXTI/UART0_TX(RX)/SPI_DI(DO)/SDA/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	IO	Pull up/External interruption/UART0 TX(RX)/SPI_DI(DO)(DO)/IIC data/Timer0 channel 0/ADC trigger signal 1/comparator 1 negative terminal input/P0.15, built-in 10k pull-up resistor that can be enabled by software
2	3		5	PULL_UP/WK/MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	IO	Pull up/Wake up/Motor PWM channel 0 low side/ UART0 TX(RX)/input of SPI/P1.0, built-in 10k pull-up resistor that can be enabled by software
2	3	6	6	PULL_UP/ADC_CH11/OPAx_OUT/LDO15/P2.7	IO	Pull up/ADC channel 11/OPAx output/LDO15 output/P2.7, built-in 10k pull-up resistor that can be enabled by software
3		7	7	LDO5V	Power Source	Chip 5V LDO output pin, external 1uF decoupling capacitor, and as close as possible to LDO5V pin
4	4	8	8	VCC	Power Source	Chip medium voltage power supply, power supply range 7.5 ~ 32V. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of chip, and the chip does not need to sleep, it is recommended to add a 1k~2k ohm shunt resistor between VCC and AVDD. Refer to Chapter 19 for specific resistance calculation. There must be a decoupling capacitor greater than or equal to 1uF between VCC pin and ground
5	5	9	9	HO1	Output	The A-phase PWM high-drive output is controlled by the PWM output function of MCU P1.7 port. For the MCPWM_SWAP=1 with the configured address 0x4001_1C7C, see user manual for details
6	6	10	10	LO1	Output	The A-phase PWM low-drive output is controlled by the PWM output function of MCU P1.4 port. A 51 ohm resistor must be connected between LO1 output and the gate of the MOS tube
7	7	11	11	HO2	Output	The A-phase PWM high-drive output is controlled by the output signal of MCU P1.8 port.
8	8	12	12	LO2	Output	The B-phase PWM low-drive output is controlled by the PWM output function of MCU P1.5 port. A 51 ohm resistor must be connected between LO2 output and the gate of the MOS tube
9	9	13	13	HO3	Output	The C-phase PWM high-drive output is controlled by the PWM output function output signal of MCU P1.9 port.
10	10	14	14	LO3	Output	The C-phase PWM low-drive output is controlled by the PWM output function of MCU P1.6 port. A 51 ohm resistor must be connected between LO3 output and the gate of the MOS tube
		15	15	GND	GND	Ground Pin. It's strongly recommended to connect all the Ground Pin together on PCB
		16	16	OPA0_IP/P1.14	IO	Op amp 0 positive input/P1.14
		17	17	OPA0_IN/P1.15	IO	Op amp 0 negative input/P1.15
11	11		17	PULL_UP/SPI_DI(DO)/SCL/ADC_CH9/CMP0_IP0/P2.9	IO	Pull up/SPI_DI(DO)(DO)/IIC clock/ADC channel 9/comparator 0 positive terminal input channel 0/P2.9, built-in 10k pull-up resistor that can be enabled by software
11	11	18	18	OPA1_IN/P0.9	IO	Op amp 1 negative input/P0.9

12	12	19	19	OPA1_IP/P0.10	IO	Op amp 1 positive input/P0.10
			19	PULL_UP/SPI_CLK/ADC_CH8/CMP1_IP0/P2.1	IO	SPI clock/ADC channel 8/comparator 1 positive terminal input channel 0/P2.1, built-in 10k pull-up resistor that can be enabled by software
12	12	19	20	CMP1_OUT/REF/MCPWM_BKIN0/SPI_CS/TIM0_CH1/P2.3	IO	Comparator 1 output/voltage reference signal/motor PWM termination signal 0/SPI chip selection signal/P2.3
12	12	20	20	PULL_UP/CMP0_OUT/HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CMP1_IP1/P2.4	IO	Comparator 0 output/Hall sensor A phase input/motor PWM channel 2 high side/UART1 TX(RX)/Timer1 channel 0/ADC trigger signal 3/comparator 1 positive input channel 1/P2.4, built-in 10k pull-up resistor that can be enabled by software
	13	20	21	PULL_UP/CMP1_OUT/HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/P2.5	IO	Comparator 1 output/Hall sensor B phase input/motor PWM channel 2 low side/UART1 TX(RX)/Timer1 channel 1/ADC trigger signal 0/comparator 1 positive terminal input channel 2/P2.5, built-in 10k pull-up resistor that can be enabled by software
13	14	21	22	PULL_UP/HALL_IN2/MCPWM_CH3P/TIM3_CH0/ADC_TRIG1/CMP1_IP3/P2.6	IO	Hall sensor C phase input/motor PWM channel 3 high side/Timer3 channel 0/ADC trigger signal 1/comparator 1 positive input channel 3/P2.6, built-in 10k pull-up resistor that can be enabled by software
13	14	21	22	PULL_UP/SWCLK/MCPWM_CH3N/UART0_TX(RX)/SCL/TIM3_CH1/P2.13	IO	SWD clock/motor PWM channel 3 low side/UART0 TX(RX)/IIC clock/Timer3 channel 1/P2.13, built-in fixed pull-up 10k resistor
14	15	22	23	PULL_UP/SWDIO/UART0_TX(RX)/SDA/TIM2_CH1/P2.0	IO	SWD data/UART0 TX(RX)/IIC data/Timer2 channel 1/P2.0, built-in fixed pull-up 10k resistor
14	15	23	24	PULL_UP/WK/EXTI/ADC_CH4/DAC_OUT/P0.0	IO	Pull up/wake up/External interruption/ADC channel 4/DAC output/P0.0, built-in 10k pull-up resistor that can be enabled by software
15	16	23	24	PULL_UP/EXTI/RSTN/SPI_DI(DO)/P0.2	IO	Pull up/External interruption/RSTN/SPI input/P0.2, used as RSTN by default, a 10nF~100nF capacitor externally connected to the ground, and a 100k pull-up resistor inside. It is recommended to place a 10k-20k pull-up resistor between RSTN and AVDD on the PCB. If there is a pull-up resistor externally, the capacitance of RSTN is fixed to be 100nF.
16		24		GND	GND	Ground Pin. It's strongly recommended to connect all the Ground Pin together on PCB

Table 3-2 LKS32MC05x with Built-in 3P3N Driver Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0	GPIO
P0.0										ADC_CH4, DAC_OUT	PULL_UP/WK/EXTI
P0.1											
P0.2					SPI_DI(DO)						PULL_UP/EXTI
P0.3						SCL		TIM2_CH0		ADC_CH7	
P0.4						SDA		TIM2_CH1		ADC_CH13	
P0.5										ADC_CH12	
P0.6				UART1_TX(RX)			TIM1_CH0				
P0.7				UART1_TX(RX)			TIM1_CH1				
P0.8											
P0.9										OPA1_IP	
P0.10										OPA1_IN	
P0.11		HALL_IN0				SCL		TIM3_CH0		ADC_CH6/CMP0_IP1	PULL_UP/EXTI
P0.12		HALL_IN1				SDA		TIM3_CH1		ADC_CH2/CMP0_IP2	PULL_UP/EXTI
P0.13		HALL_IN2								ADC_CH3/CMP0_IP3	EXTI
P0.14	CMP0_OUT		MCPWM_BKIN1	UART0_TX(RX)	SPI_CLK	SCL	TIM0_CH1		ADC_TRIG0	ADC_CH10/CMP0_IP4	PULL_UP/EXTI
P0.15			MCPWM_CH0P	UART0_TX(RX)	SPI_DI(DO)	SDA	TIM0_CH0		ADC_TRIG1	CMP0_IN	PULL_UP/EXTI

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0	GPIO
P1.0			MCPWM_CH0N	UART0_TX(RX)	SPI_DI(DO)						PULL_UP/WK
P1.1					SPI_CS					OPA2_IP	WK
P1.2								TIM3_CH0		OPA2_IN	
P1.3								TIM3_CH1		ADC_CH5	
P1.4	LRC		MCPWM_CH0P								
P1.5	HRC		MCPWM_CH0N								
P1.6			MCPWM_CH1P								
P1.7			MCPWM_CH1N								
P1.8			MCPWM_CH2P								
P1.9			MCPWM_CH2N								
P1.10			MCPWM_CH3P	UART0_TX(RX)		SCL	TIM0_CH0		ADC_TRIG2		
P1.11			MCPWM_CH3N	UART0_TX(RX)		SDA	TIM0_CH1		ADC_TRIG3		
P1.12											
P1.13					SPI_CLK		TIM0_CH0				
P1.14										OPA0_IP	
P1.15										OPA0_IN	

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0	GPIO
P2.0				UART0_TX(RX)		SDA		TIM2_CH1			PULL_UP
P2.1					SPI_CLK					ADC_CH8/CMP1_IP0	PULL_UP
P2.2										CMP1_IN	
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			REF	
P2.4	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART1_TX(RX)			TIM1_CH0		ADC_TRIG3	CMP1_IP1	PULL_UP
P2.5	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART1_TX(RX)			TIM1_CH1		ADC_TRIG0	CMP1_IP2	PULL_UP
P2.6		HALL_IN2	MCPWM_CH3P					TIM3_CH0	ADC_TRIG1	CMP1_IP3	PULL_UP
P2.7										ADC_CH11/OPAx_OUT/LDO15	PULL_UP
P2.8				UART0_TX(RX)	SPI_DI(DO)			TIM2_CH0			
P2.9					SPI_DI(DO)	SCL				ADC_CH9/CMP0_IP0	PULL_UP
P2.10					SPI_DI(DO)	SDA					
P2.11			MCPWM_CH1P					TIM2_CH0			
P2.12			MCPWM_CH1N		SPI_CS			TIM2_CH1	ADC_TRIG2		
P2.13			MCPWM_CH3N	UART0_TX(RX)		SCL		TIM3_CH1			PULL_UP
P2.14					SPI_DI(DO)	SCL				OPA3_IP	
P2.15					SPI_CS	SDA				OPA3_IN	

4 Package Size

4.1 LKS32MC057EM6S8/ LKS32MC057FM6S8

SSOP24L:

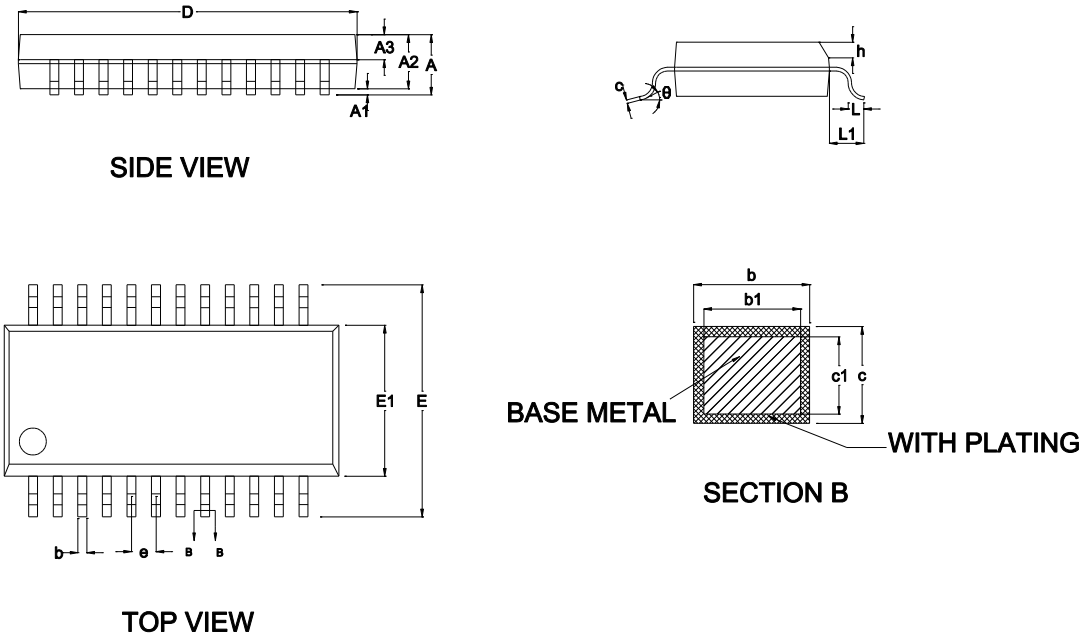

Fig. 4-1 LKS32MC057EM6S8 Package Diagram

Table 4-1 LKS32MC057EM6S8 Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

4.2 LKS32MC055DL6S8

SOP16L

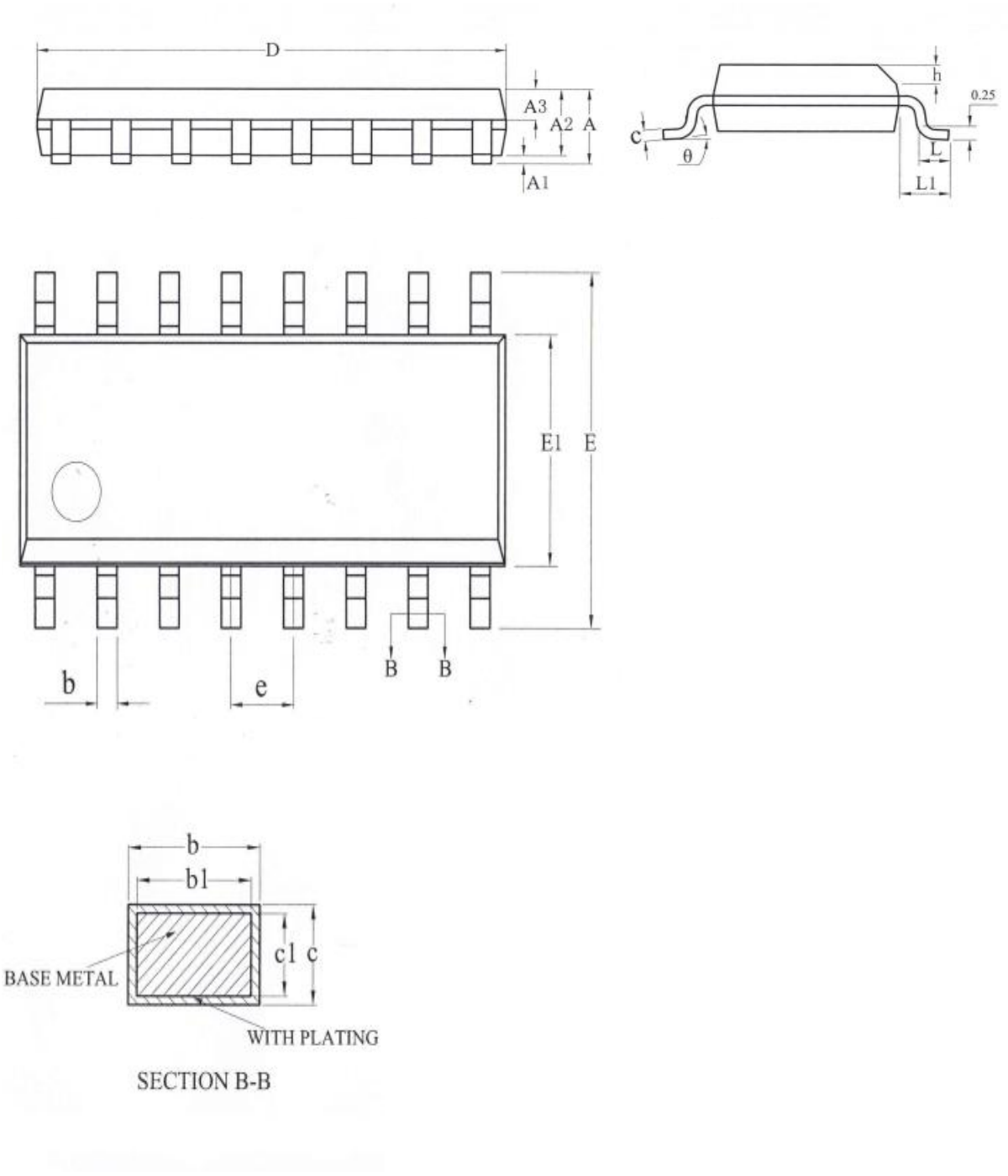

Fig. 4-2 LKS32MC055DL6S8 Package Diagram

Table 4-2 LKS32MC055DL6S8 Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225

Package Size

A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
b1	0.38	0.41	0.44
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.15	2.25	2.35
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

4.3 LKS32MC055EL6S8

ESOP16L

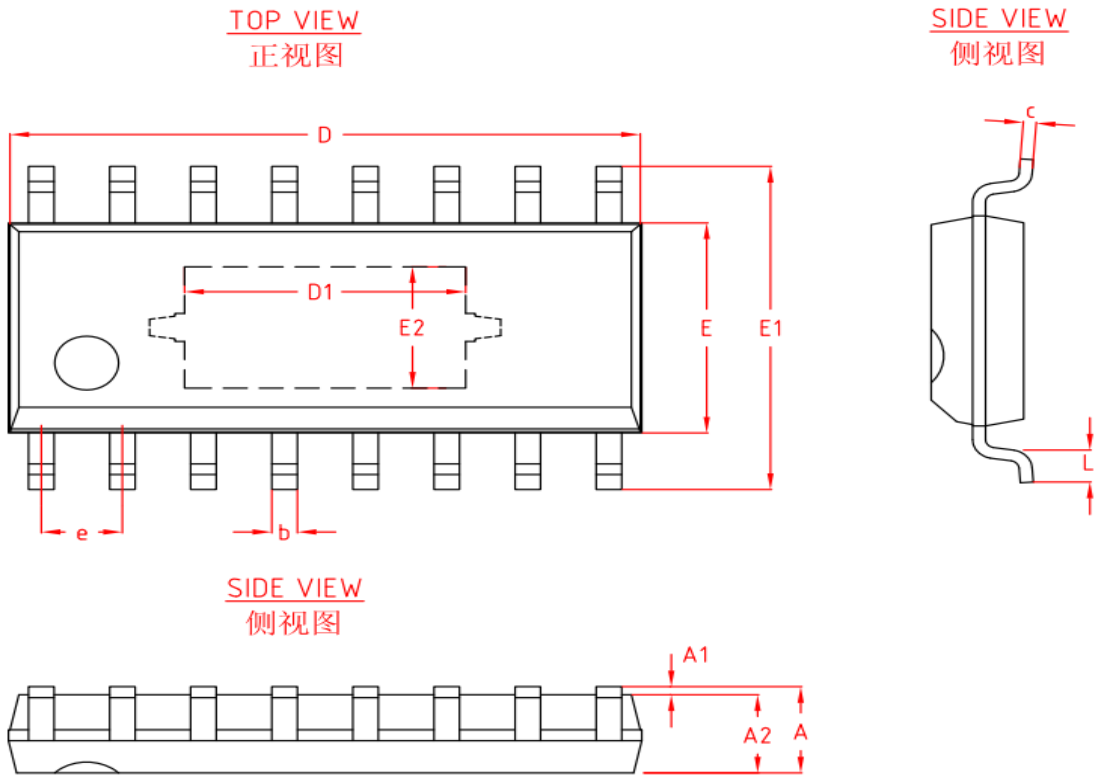

Fig. 4-3 LKS32MC055EL6S8 Package Diagram

Table 4-3 LKS32MC055EL6S8 Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75

A1	0.05	-	0.18
A2	1.35	1.45	1.55
b	0.35	-	0.50
c	0.19	-	0.25
D	9.80	10.00	10.20
D1	4.3	4.4	4.5
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
E2	2.15	2.25	2.35
e	1.27 BSC		
L	0.40	-	0.80

5 Electrical Characteristics

Table 5-1 LKS32MC05x with Built-in 3P3N Driver Electrical Absolute Characteristics

Parameter	Min	Max.	Unit	Description
MCU Power Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Power Supply Voltage (VCC)	-0.3	+40.0	V	Gate driver power supply
5V LDO output current		40	mA	
Operating Temperature	-40	+105	˚C	
Storage Temperature	-40	+150	˚C	
Junction Temperature	-	125	°C	
Pin Temperature	-	260	°C	Soldering for 10 seconds

Table 5-2 LKS32MC05x with built-in 3P3N driver Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
MCU Power Supply Voltage (AVDD)	2.2	5	5.5	V	
Analog Supply Voltage ($AVDD_A$)	2.8	5	5.5	V	
Gate Driver Supply Voltage (VCC)	7.5		32	V	3P3N Gate driver power supply

OPA could work under 2.2V, but the output range will be limited.

Table 5-3 LKS32MC05x ESD parameters

Item	Min.	Max.	Unit
ESD test (HBM)	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC05x Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

Table 5-5 LKS32MC05x with Built-in 3P3N Driver IO Absolute Characteristics

Parameter	Description	Min.	Max.	Unit
$V_{IN-GPIO}$	GPIO Signal Input Voltage Range	-0.3	6.0	V
I_{INJ_PAD}	Maximum Injection Current of a Single GPIO	-11.2	11.2	mA
I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 5-6 LKS32MC05x with Built-in 3P3N Driver IO DC Parameters

Parameter	Description	AVDD	Conditions	Min.	Max.	Unit
V_{IH}	High input level of digital IO	5V	-	3.04		V
		3.3V		2.04		
V_{IL}	Low input level of digital IO	5V	-		0.3*AVDD	V
		3.3V			0.8	
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD		V
		3.3V				
I_{IH}	Digital IO current consumption when input is high	5V	-		1	uA
		3.3V				
I_{IL}	Digital IO current consumption when input is low	5V	-	-1		uA
		3.3V				
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8		V
V_{OL}	Low output level of digital IO		Current = 11.2mA		0.5	V
R_{pup}	Pull-up resistor*			8	12	kΩ
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit			100	200	Ω
C_{IN}	Digital IO Input-capacitance	5V	-		10	pF
		3.3V				

*Only some IOs have built-in pull-up resistors, see section “Pin Function Description” for details.

Table 5-7 LKS32MC05x Module Current/IDD

Module	Min	Typ	Max	Unit
CMP x1		0.005		mA
OPA x1		0.400		mA
ADC		1.510		mA
DAC		0.710		mA
Temp Sensor		0.150		mA
Band-Gap		0.154		mA
4MHz RC Clock		0.105		mA
PLL		0.080		mA
CPU+flash+SRAM (96MHz)		6.867		mA
CPU+flash+SRAM (12MHz)		1.300		mA
CRC		0.070		mA
UART		0.107		mA
MCPWM		0.053		mA
TIMER		0.269		mA
SPI		0.500		mA

IIC		0.500		mA
Sleep Mode	10	30	50	uA

The above tests, if not specifically marked, are all powered at room temperature 25° 5V, using 96MHz clock operating conditions, due to the manufacturing process there are device model deviations, the current consumption of different chips will have individual differences.

6 Analog Characteristics

Table 6-1 LKS32MC05x with Built-in 3P3N Driver Analog Characteristics

Parameter	Min	Typ	Max	Unit	Description
ADC					
Power supply	2.8	5	5.5	V	
Sampling rate		3		MHz	$f_{adc}/16$
Differential Input Signal Range	-2.4 +0.048		+2.4 -0.048	V	When Gain=1;REF=2.4V
	-3.6 +0.072		+3.6 -0.072	V	When Gain=2/3;REF=2.4V
Single-ended Input Signal Range	-0.3		AVDD+ 0.3	V	Limited by the input voltage of the IO port
The differential signal is usually the signal output from the OPA inside the chip to the ADC; Single-ended signals are typically sampled externally via an I0 input: The ADC should measure the signal amplitude no more than ±98% of the full scale, regardless of the internal/external reference used. In particular, when using an external reference, it is recommended that the sampling conductor not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	500k			Ohm	
Input Capacitance		10pF		F	
Reference Voltage (REF)					
Power supply	2.2	5	5.5	V	
Output Deviation	-9		9	mV	
Power supply rejection ratio(PSRR)		70		dB	
Temperature coefficient		20		ppm/°C	
Output voltage		1.2		V	
DAC12					
Power supply	2.2	5	5.5	V	
Load Resistance	50k			Ohm	
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0 .1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	

Parameter	Min	Typ	Max	Unit	Description
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational Amplifier (OPA)					
Power supply	3.1	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load Resistance	20k			Ohm	
Load capacitance			5p	F	
Input common-mode range	0		AVDD	V	
Output Common Mode Voltage Range	0.1		AVDD-0.1	V	Under minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification xOFFSET
Common Mode Voltage (Vcm)	1.65	1.9	2.2	V	Measurement condition: normal temperature. Operational amplifier swing =2× min(AVDD-Vcm, Vcm). You are advised to measure the Vcm and correct software subtraction after powering on applications that use OPA single-end output. For more analysis, please refer to the official website application note ANN009-Differences between Opamp Differential and Single-end Operating Modes.
Common Mode Rejection Ratio (CMRR)		80		dB	
Power Supply Rejection Ratio (PSRR)		80		dB	
Load Current			500	uA	
Slew rate		5		V/us	
Phase Margin (PM)		60		Degree	
Comparator (CMP)					

Parameter	Min	Typ	Max	Unit	Description
Power supply	2.2	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET		-19.2		mV	0 mV hysteresis, CMP output transitions from low to high
		-22.4		mV	0 mV hysteresis, CMP output transitions from high to low
		-18.4		mV	20 mV hysteresis, CMP output transitions from low to high
	-	8.1		mV	20 mV hysteresis, CMP output transitions from high to low
Delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		10		mV	HYS='0'
		0		mV	HYS='1'

Description of Analog Register Table:

Address space of 0x40000040 to 0x40000050 are the calibration registers of each analog module. These registers will be set to a unique calibration value in factory. Generally, users are advised not to configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x40000020 to 0x4000003c are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers will be configured according to the actual application scenarios.

7 Power Management System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

The chip is powered by a 7.5V ~ 32V single supply to save the power supply costs outside the chip. An internal LDO5 supply the power of MCU. And all internal digital circuits and PLL modules in the MCU are powered by an internal LDO15.

For the 055D, 057E and 057F product, AVDD is the low-voltage power supply with a power supply range of 2.2~5.5V. In applications with good heat dissipation conditions, it can be directly connected to the LDO5V pin of the chip. To reduce the system power consumption and use the 5V power supply generated by an external DC or charge pump, connect this pin to the external 5V power supply

For the 055E product, AVDD is the output pin of chip 5V LDO and the chip shall be connected with a 1uF decoupling capacitor, and it should be as close as possible to the LDO5V pin.

The LDO15 automatically turns on after power-on, without software configuration, and the LDO output voltage can be adjusted through software.

The output voltage of LDO15 can be adjusted by setting register LDO15TRIM <2:0>. The corresponding value of the register can be seen in the analog register table. LDO15 has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again. If fine-tuning of the LDO output voltage is required, please read the original configuration value first, and then add the configuration value corresponding to the fine-tuning amount to the register.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.1V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation

8 Clock System

The clock system consists of a 64KHz RC oscillator, an internal 4MHz RC oscillator and a PLL.

The 64k RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode. The 4MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz.

Both 64k and 4M RC clocks will been through factory calibration, in the range of -40 ~ 105 ℃, the accuracy of the 64K RC clock is ± 50%, and the accuracy of the 4M RC clock is ± 1%.

The 4M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 4M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 4M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be also turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and enabled by software.

9 Bandgap Voltage Reference

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = ’0’. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

The voltage reference can be measured by setting REF_AD_EN = ’1’ and via IO P2.3.

10 ADC module

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 4M RC clock and PLL should be turned on first, and the operating frequency of ADC should be selected. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

f_{adc} ADC takes 16 ADC clock cycles to complete one conversion, of which 12 are conversion cycles and 4 are sampling cycles. i.e. = f_{conv} /16. When the ADC clock is set to 48MHz, the conversion rate is 3Msps. The sampling cycle can be set by configuring the SAMP_TIME register in SYS_AFE_REG7. It is required to be set to more than 6 (including 6), i.e., the sampling time of 10 ADC clk or more.
The recommended value is 8, which corresponds to the ADC output data rate of 2MHz.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, one-time 1 to16 channels scanning mode, continuous 1 to 16 channels scanning mode. It has a set of 16 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

The ADC has two gain modes, which are set by GAIN_SHAx, corresponding to 1x and 2/3 x gain setting. 1x gain corresponds to an input signal range of ± 2.4V, and 2/3 gain corresponds to an input signal range of ± 3.6V. When measuring the output signal of the OPA, select the specific ADC gain according to the maximum signal that the OPA may output.

11 Operational Amplifier

2-channel of rail-to-rail OPAs are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 2-channels amplifiers by setting OPAOUT_EN <1:0>, and send it to the P2.7 IO port through a buffer for measurement. Because of the BUFFER, the operational amplifier is also able to send one output signal in the normal working mode.

When the chip is powered on, the amplifier module is OFF by default. It can be turned on by setting OPAxPDN = '1', and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes that are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 2-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay can be set to 0.15 us, and can be set to be less than 30 ns. The hysteresis voltage can be set to 20mV/0mV by CMP_HYS.

The signal sources of the positive and negative inputs can be programmed by register CMP_SELP<2:0> and CMP_SELN<1:0>. For details, please refer to the analog register description.

When the chip is powered on, the comparator module is OFF. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

13 Temperature Sensor

The chip has a temperature sensor with an accuracy of ±2°C. The operating temperature of chips will be corrected before leaving the factory, and the corrected value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = ’1’, and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 Digital-to-analog Converter (DAC) Module

The chip has a 1-channel 12 bit DAC, and the maximum range of the output signal can be set to 1.2V/4.8V through the register DAC_G.

The 12bit DAC can be output via IO port P0.0 by setting register DACOUT_EN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output code rate of the DAC is 1MHz.

When the chip is powered on, the DAC module is OFF. DAC can be turned on by setting DAC12BPDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor Core

- 32-bit Cortex-M0 + DSP dual-core processor
- 2-wire SWD debug pin
- System frequency is up to 96MHz

16 Storage

16.1 Flash

- Built-in flash including 32kB/64kB main storage area and 1kB NVR
- Available for repeated erasure and writing for at least 20,000 times
- Data retention at room temperature 25℃ for up to 100 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size is 512 bytes. The data can be erased and written according to Sector. It supports runtime programming.
- Flash data anti-theft (any value other than 0xFFFFFFFF must be written to the last word)

16.2 SRAM

- Built-in 2.5kB SRAM

17 Motor Control PWM

- MCPWM operating frequency is up to 96MHz
- Supports up to 4 channels of complementary PWM output with adjustable phase
- The width of dead-zone in each channel can be configured independently
- Support edge-aligned PWM mode
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simultaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support 4-channel capture mode for measuring external signal/pulse width
- Support 4-channel comparison mode for timed interruption of edge-aligned PWM

19 Hall Sensor Interface

- Built-in 1024 cycles filtering at most
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 General Peripherals

- Two UART, full-duplex operation, support 7/8 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, the reset time ranges from 0.064s to 32s, the minimum step size is 0.064s.

21 Three-phase P/N MOS Gate Drive Module

21.1 Module parameter

Table 21-1 LKS32MC057EM6S8 Driver Module Parameters

Symbol	Parameter	Condition	Min	Typical	Max.	unit
Static parameters						
VCC_ON	VCC undervoltage recovery voltage		5.8	6.5	7.4	V
VCC_UVLO	VCC undervoltage threshold voltage		5.4	6	6.8	V
VCC_HYS	Undervoltage hysteresis		0.3	0.5	0.8	V
IQC	Static power supply	VIN=0V	0.3	0.5	1.0	mA
VDD	5V LDO output voltage		4.7	5.0	5.3	V
VIH	Logic '1' flip voltage		2.2			V
VIL	Logic '0' turnover voltage				0.6	V
I_SOURCE	Input signal logic '1' bias current	VIN=5V		32	100	uA
I_SINK	Input signal logic '0' bias current	VIN=0V			1	uA
V_{HO}	HOx(x=1~3) output turn-on voltage (because HO drives PMOS, low level corresponds to the turn-on)		VCC-11	VCC-10	VCC-8.5	V
V_{LO}	LOx(x=1~3) output turn-on voltage		8.5	10	11.5	V
I_{HO+}	HOx(x=1~3) output source current	HOx=VCC-10V	-	300	-	mA
I_{HO-}	HOx(x=1~3) input sink current	HOx=VCC	-	35	-	mA
I_{LO+}	LOx(x=1~3) output source current	LOx=0V	-	60	-	mA
I_{LO-}	LOx(x=1~3) input sink current	LOx=10V	-	300	-	mA
T_{SD}	TSD temperature		-	150	-	℃
$T_{RECOVER}$	TSD recovery temperature		-	135	-	℃
I_{Ldo}	Power supply capacity			40		mA
Dynamic parameters (CL=1nF)						
T_{ON}	Turn-on delay		-	80	-	ns

T_{OFF}	Turn-off delay		-	30	-	
TH_R	HOx rise time		-	50	-	
TH_F	HOx falling time		-	400	-	
TL_R	LOx rise time		-	200	-	
TH_F	LOx falling time		-	50	-	
DT	Built-in dead-zone time		-	100	-	

The input and output waveforms of the P/N MOS drive module are as shown below. As shown in the figure, HIN/LIN is the output signal of the MCPWM module inside the chip. For HIN, the output high level corresponds to the HO output low level, thereby driving the high-drive PMOS to turn on. For LIN, the output high level corresponds to the LO output high level, thereby driving the low-drive NMOS to turn on. Therefore, the polarity selection of P and N in MCPWM register MCPWM_IO01/MCPWM_IO23 does not need to be reversed.

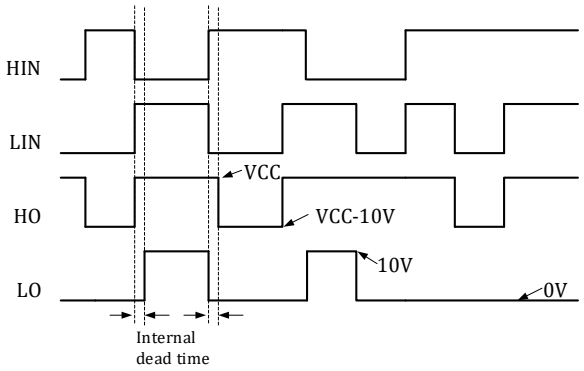

Fig. 21-1 Drive Module Input and Output Timing Sequence Waveform

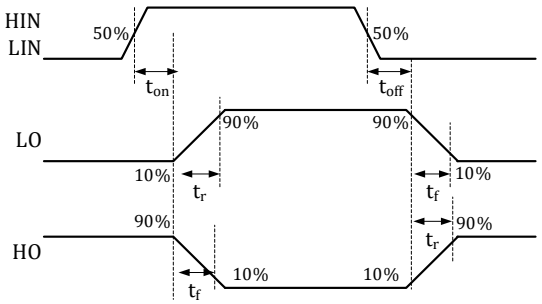

Fig. 21-2 Drive Module Output Change Edge Timing Waveform

21.2 Recommended Application Diagram

The output pin signal of the driver module LO1/HO1 corresponds to MCPWM function output of GPIO P1.4/P1.7, LO2/HO2 corresponds to MCPWM function output of GPIO P1.5/P1.8, and LO3/HO3 corresponds to MCPWM function output of GPIO P1.6/P1.9.

The MCPWM_SWAP register must be set for the integrated predrive chip, otherwise the PWM

cannot be output normally. Write 0x67 to such register to write BIT[0] to 1, and write other values to write BIT[0] to 0. When the value of MCPWM_SWAP is 1, it is used to include the pre-drive chip application environment. The sequence is converted within the logic to facilitate the interconnection of the chip and the drive chip. In general applications, only three sets of MCPWM channels are required, so only three sets of sequences are converted.

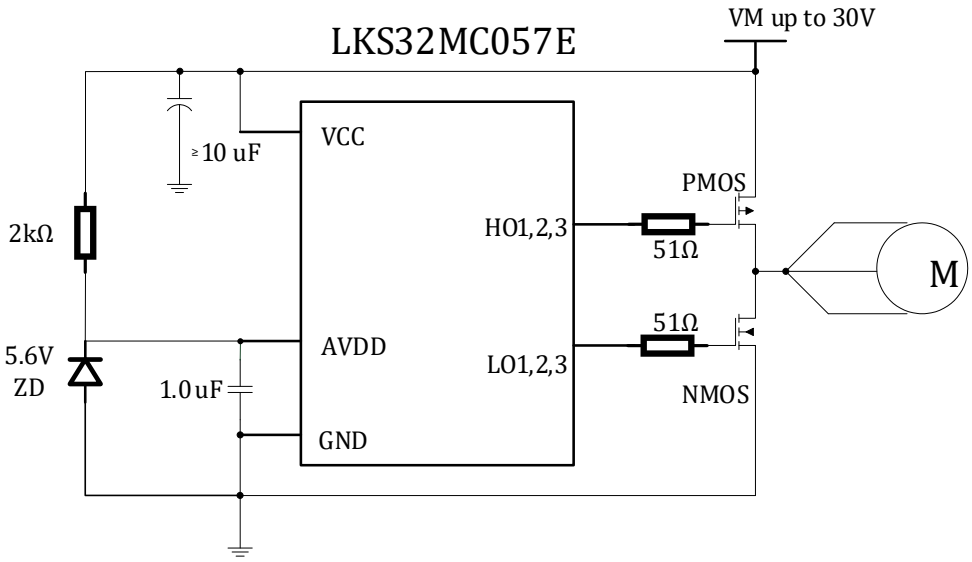

Fig. 21-3 LKS32MC055DL6S8/ LKS32MC055EL6S8/LKS32MC057EM6S8 Typical Drive Module Application Diagram

The output pin signal LO1/HO1 of the drive module corresponds to the MCPWM function output of corresponding GPIO P1.4/P1.7, LO2/HO2 corresponds to the MCPWM function output of corresponding GPIO P1.5/P1.8, and LO3/HO3 corresponds to the MCPWM function output of the corresponding GPIO P1.6/P1.9. However, the address to be configured is MCPWM_SWAP=1 of 0x4001_1C7C. See the user manual for details.

A 51ohm resistor is recommended between LO1/2/3 and the NMOS gate, HO1/2/3 and the PMOS gate when phase current is larger than 2A.

In applications where VCC is higher than 20V, the AVDD pin is powered by the chip's own LDO5V pin, and the chip does not need to sleep, it is recommended to add a 1k~2k ohm shunt resistor between VCC and AVDD. This resistor is connected between the input and output terminals of internal 5V LDO to share the partial heat dissipation function. The resistor needs to be placed at a distance from the chip (for 055D and 057E, if the AVDD pin is powered by an external 5V power supply, this resistor is not required).

The calculation of resistance value must be based on the following formula:

R>=(VCC-AVDD)/I

Whereof, I is the total power consumption on the 5V power supply, including the power

consumption of the MCU and the power consumption of 5V peripheral device (e.g., HALL).

In case an external shunt resistor is connected, a 5.6V voltage regulator tube should be mounted on the AVDD pin.

Meanwhile, in applications where a resistor is connected between VCC and AVDD, please note that the RC constant on RSTN should not be too large. It is recommended to keep the RC constant to be 1ms. I.e., in case the external resistance of the chip is not added to 5V, when the internal pull-up resistance is 100k, the capacitance on RSTN is selected as 10nF. If a 10k or 20k pull-up resistor is added externally, the capacitance on RSTN is selected as 100nF.

There must be a decoupling capacitor ≥10uF between VCC pin and ground. Filtering capacitors or ESD diodes are needed to ensure that the power-on overshoot does not exceed the VCC limit withstand voltage.

22 Special IO Multiplexing

Notes for Special IO Multiplexing of LKS05x

The SWD protocol includes two signals: SWCLK and SWDIO. The former is a clock signal. To the chip, it is an input and will always be an input. The latter is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Users could use two IOs of SWD as GPIOs. The IO SWCLK could be multiplexed by P2.13, and the IO SWDIO could be multiplexed by P2.0. The precautions are as follows:

- The default state of multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[6] to enable multiplexing. I.e., after the hard reset of the chip, the initial state of IO s are SWD. Both IOs of SWD shall be provided with pull-up resistors inside the chip (the internal pull-up resistor of the chip is about 10K). When the IOs are used as SWD functions, the pull-up resistors are turned on by default and cannot be turned off. When IO is used as GPIO, the pull-up resistor can be controlled by GPIO2_PUE[13] and GPIO2_PUE[0]. P2.0 and P2.13 are forced to be used as SWD function within the 30ms after chip power-on reset. The software can write 1 to SYS_RST_CFG[6], but IO function switching won't take effect before 30ms after POR. The 30ms is counted by LRC. There is certain deviation due to the process reason.
- After multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. The greater margin means the greater probability of the successful one-time erasion.
- Secondly, the program should include a multiplexing exit mechanism. For example, a change in some other IO level (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In the packages of SSOP24L, QFN5*5 40L-0.75 and SOP16L, SWDIO may be directly bonded with P0.0, SWCLK may be directly bonded with P2.6. When P2.6 and SWCLK are bonded together, it is generally recommended to multiplex SWCLK as P2.13 to prevent SWCLK from always being in the input state, which will cause SWCLK to malfunction when the P2.6 signal changes.

If only SWCLK is multiplexed at this time, and SWDIO is not multiplexed, the precautions are the same as above.

For RSTN signal, the default is for the external reset pin of LKS05x chip.

LKS05x can realize the function of RSTN multiplexing as other IOs, and the multiplexed IO is P 0.2.

The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

23 Ordering Information

Tray Package:

Package Type	Quantity per disc/tube	Quantity in box	Quantity in case
SOP16/ESOP16L	3000/ disc	6000PCS	48000PCS
SSOP24	4000/ disc	8000PCS	64000PCS
SS0P24	50/ pipe	10000PCS	4000/100000PCS
QFN 8*8	260/ disc	2600PCS	15600PCS
QFN 4*4/5*5/6*6	490/ disc	4900PCS	29400PCS
QFN 3*3	5000/ disc	5000PCS	40000PCS
LQFP48/TQFP48 0707	250/ disc	2500PCS	15000PCS
LQFP64 1010	160/ disc	1600PCS	9600PCS
LQFP100 1414	90/ disc	900PCS	5400PCS
TSSOP20/28	4000/ disc	8000PCS	64000PCS

Reel Package:

Package Type		Quantity per disc/tube	Quantity per box	Quantity boxes per case	Quantity per case
Braid -13 inches	SOP/ESOP8	4000	8000	8	64000
Braid -13 inches	SOP/ESOP16	3000	6000	8	48000
Braid -13 inches	SSOP24	4000	8000	8	64000
Braid -13 inches	TSSOP20	4000	8000	8	64000
Braid -13 inches	D/QFN3*3	5000	10000	8	80000
Braid -13 inches	D/QFN4*4	5000	10000	8	80000
Braid -13 inches	D/QFN5*5	5000	10000	8	80000
Pipe	SOP16	50	10000	10	100000
Pipe	SOP14/SSOP24	50	10000	10	100000
Pipe	TSSOP24	54	6480	6	38880

24 Version History

Table 24-1 Document Version History

Date	Version No.	Instruction
2025.08.22	1.92	Update naming rules
2025.07.22	1.91	Delete the Flash section: While one Sector is erased and written, an-other Sector can be read and accessed at the same time.
2024.08.21	1.90	Add internal predrive connection diagram
2024.08.04	1.89	Order package information updates to confirm package information by package type and package form
2023.09.25	1.88	Update welding temperature
2023.05.07	1.87	Correct I_{HO+} and I_{HO-} current values of the gate drive
2023.04.07	1.86	Update package description
2023.03.23	1.85	Modify the LSI accuracy range
2023.03.02	1.84	change Vcm 1.65~2.2
2023.02.10	1.83	Modify the P/N MOS gate driver current
2023.01.14	1.82	Add ordering information
2022.11.10	1.81	Add connection resistance between IO and internal analog circuit，change Vcm 1.7~2.2
2021.05.08	1.8	Added descriptions of UART_TX/RX and SPI_DI/DO swaps; Merge some general notes to 3.1.1 Special Notes
2021.02.06	1.7	057E/055E/055D Added the P1.0 sleep wake port
2021.01.15	1.6	Revise the pin function description of 057E
2020.12.23	1.5	Revise the driver module parameters
2020.11.30	1.4	Add the model 057F
2020.11.3	1.3	Add models 055D/055E
2020.09.16	1.2	Revise partial parameter function description
2020.08.28	1.1	OPA1 input pin polarity adjustment
2020.04.20	1.0	Initial version

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For earlier versions, please refer to this document.