Linko Semiconductor Co., Ltd.

LKS32MC05x Datasheet

1 Overview

1.1 Function

LKS32MC05x is a 32-bit MCU targeting motor control applications.

Features

- 96MHz 32-bit Cortex-M0 core
- Ultra low power sleep mode
- Industrial temperature range
- High ESD and group pulse reliability

- **Memory**
  - 32kB Flash with optional encryption to prevent hex theft, 128bit unique chip ID
  - 2.5kB RAM
- **Operating Conditions**
  - Dual power supply. The MCU is powered by 2.2V ~ 5.5V voltage, with an integrated internal LDO for the digital circuit.
  - Operating Temperature: -40~105℃
- **Clock**
  - 4MHz built-in high-precision RC oscillator, with an accuracy of ± 1% at -40 ~ 105 ℃
  - 32kHz built-in low-speed clock for low-power mode
  - Operating on an external 4MHz crystal is available
  - Internal PLL up to 96 MHz
- **Peripheral Modules**
  - Two UARTs
  - One SPI, support master-slave mode
  - One IIC, support master-slave mode
  - Two 16-bit standard timers (TIM), support capture and edge-aligned PWM function
  - Two 32-bit standard timers (TIM), support capture and edge-aligned PWM function
  - Motor control PWM module, supports 8 channels/4 pairs of PWM waveform output, independent dead-band control
  - Hall signal interface with speed measurement and debouncing function
  - Hardware watchdog
  - 3 Groups of 16bit GPIO at the most. P0.0/P0.1/P1.0/P1.1 could be used as wake-up source。P0.15 ~ P0.0 could be used as external IRQ source
- **Analog Modules**
  - 12bit SAR ADC, 3Msps sampling and conversion rate, up to 16 analog signal channels
  - Two operational amplifiers with differential PGA mode.

- Two comparators with hysteresis.
- 12bit digital-to-analog converter (DAC)
- ± 2 ℃ built-in temperature sensor
- 1.2V 0.5% built-in linear regulator
- Low-power LDO and power monitoring circuit
- RC oscillator with high precision and low temperature drift

- **Package**

Table 1-1 LKS32MC05x Package Summary

Chip	Package
LKS32MC051C6T8	TQFP48
LKS32MC052K6Q8	QFN5*5 32L-0.75
LKS32MC057M6S8	SSOP24L

1.2 Main Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 2 channels high-speed OPAs and 2 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed hight current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Support IEC/UL60730 functional security certification

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Conventions

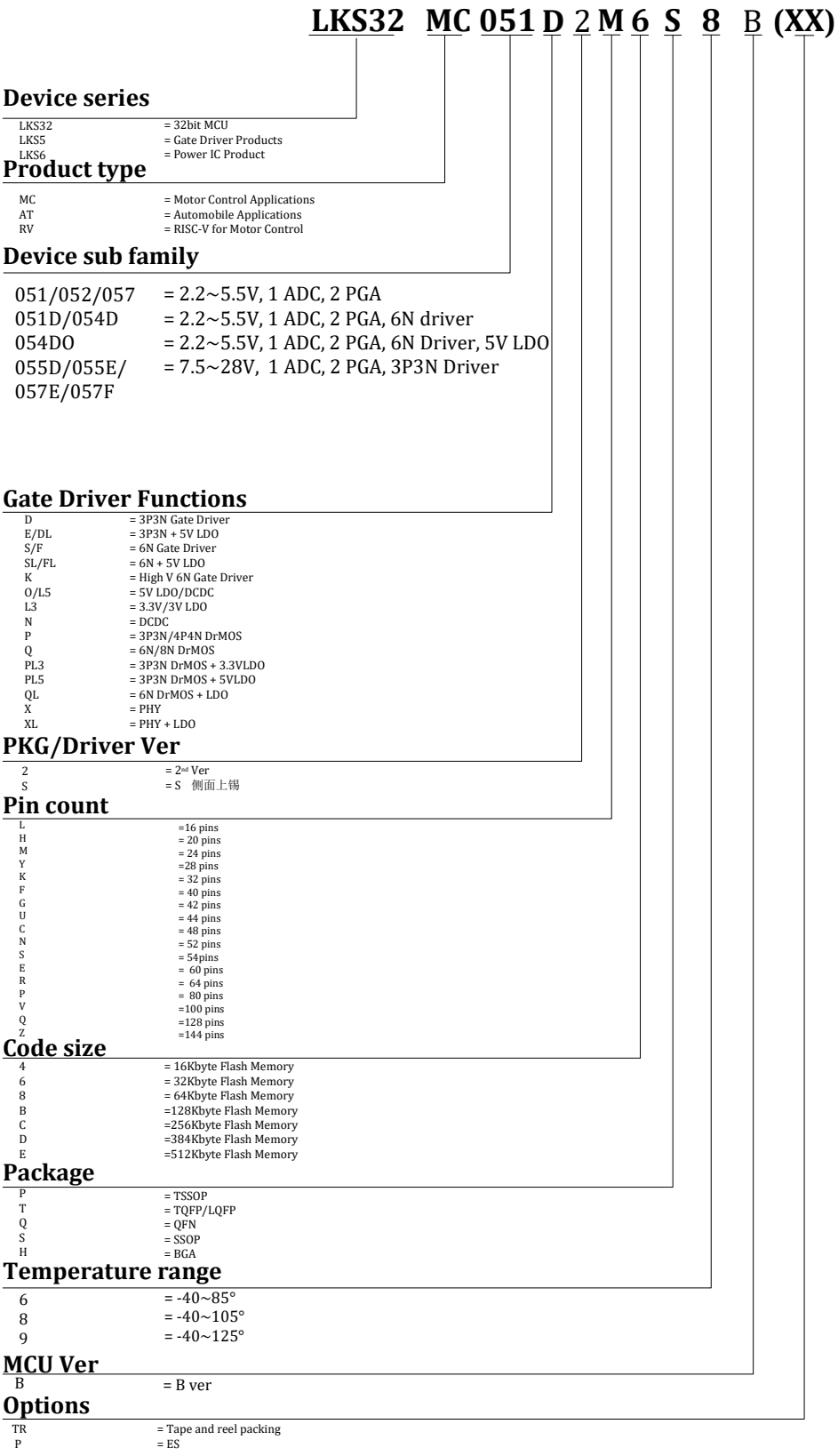

Fig. 1-1 Naming Conventions of Linko Components

1.4 Resource Diagram

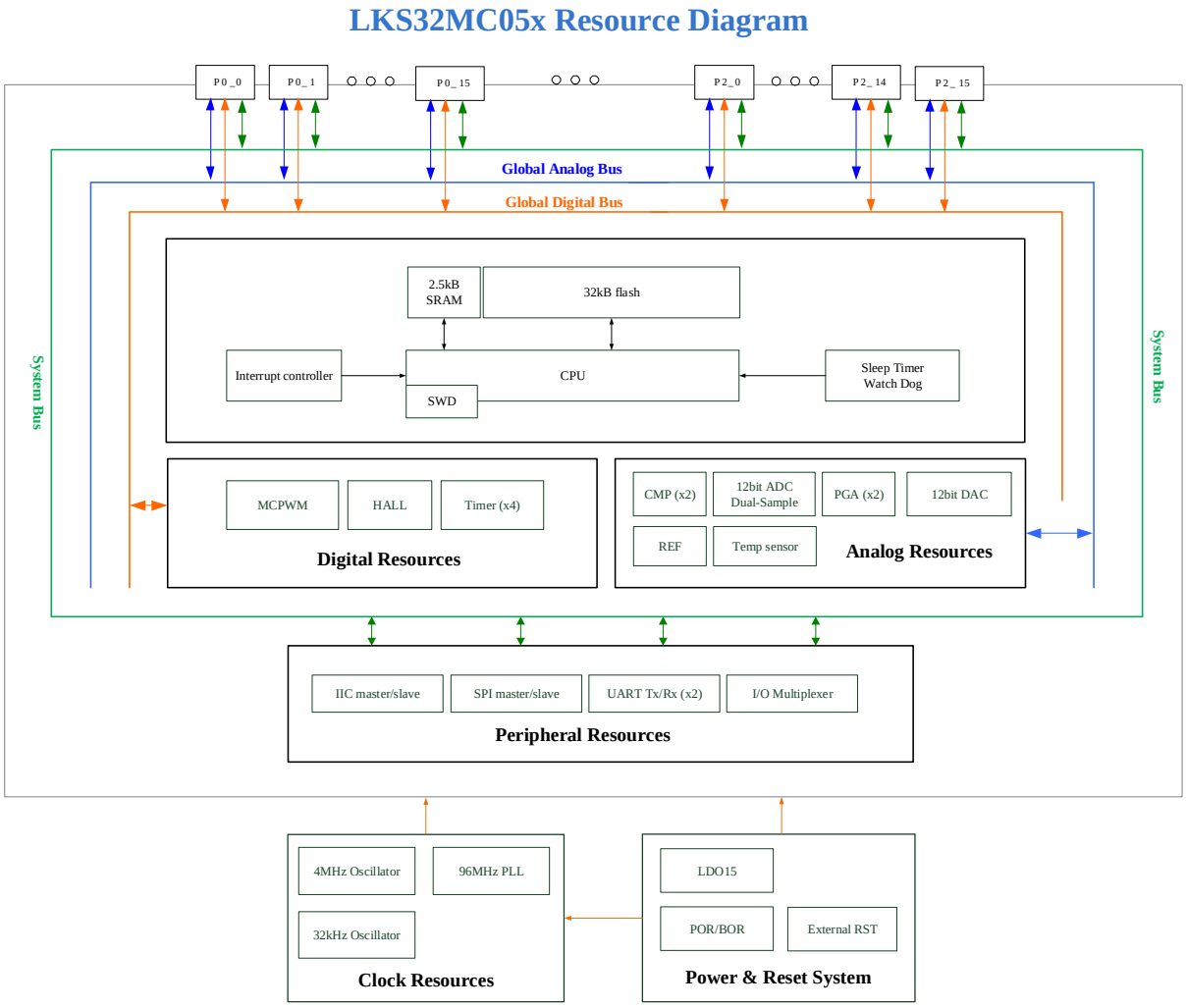

Fig. 1-2 LKS32MC05x Resource Diagram

For detail resource information of LKS32MC05x, please refer to chip selection guide.

1.5 FOC System Example

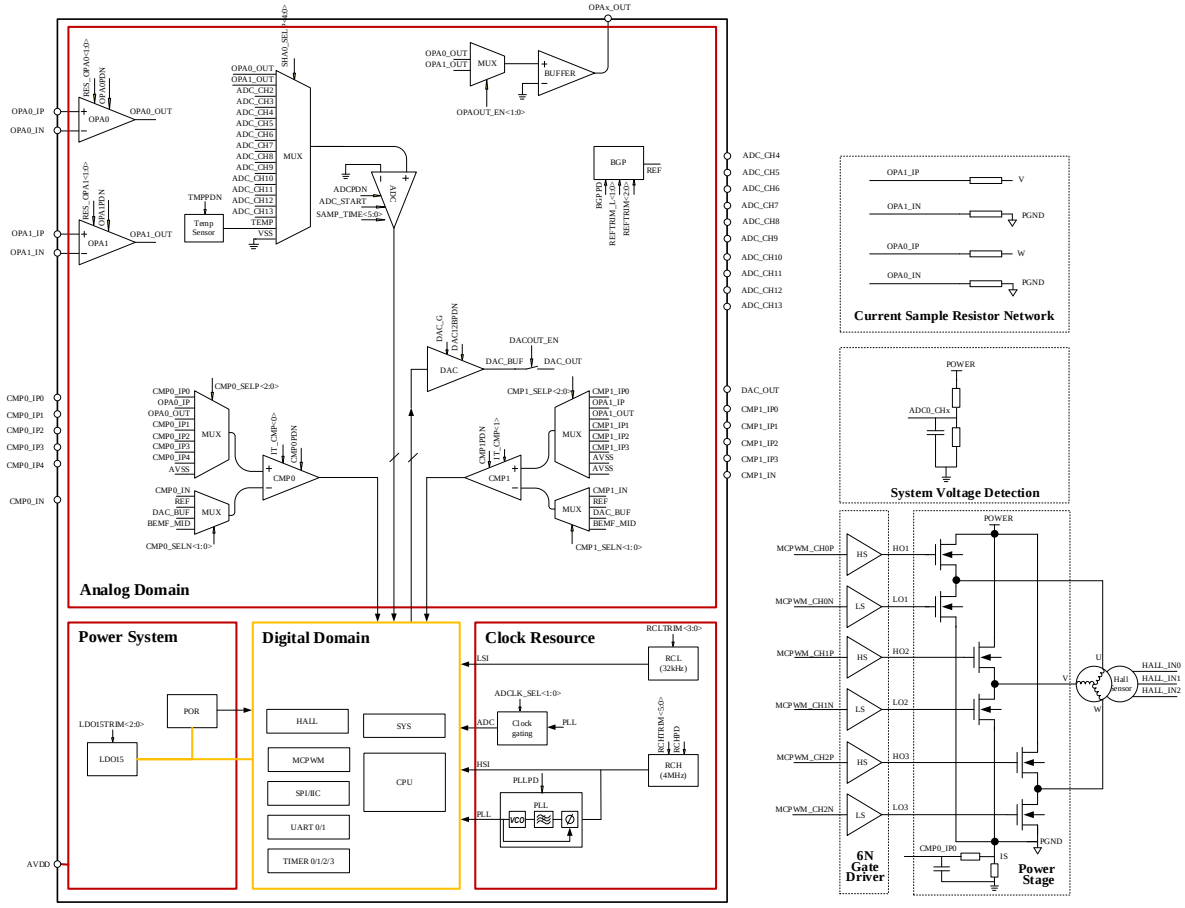

Fig. 1-3 LKS32MC05x Simplified Schematic of FOC System

2 Device Selection Guide

Table 2-1 LKS05x family device selection guide

	Freq. (MHz)	Flash (kB)	RAM (kB)	ADC Ch.	DAC	CMP	CMP Ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver Current (A)	Gate Driver Power (V)	Floating G (V)	Others	Package
LKS32MC051C6T8	96	32	2.5	12	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes							TQFP48
LKS32MC051DC6T8	96	32	2.5	11	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20	200		TQFP48
LKS32MC052K6Q8	96	32	2.5	8	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes							QFN5*5 32L-0.75
LKS32MC054DF6Q8	96	32	2.5	9	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20	200		QFN5*5 40L-0.75
LKS32MC054DOF6Q8	96	32	2.5	9	12BITx1	2	8	2	3 路	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC055DL6S8	96	32	2.5	3	12BITx1	2	4	1	1 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~28		5V LDO	SOP16L
LKS32MC055EL6S8	96	32	2.5	4	12BITx1	2	6	1	3 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~28		5V LDO	SOP16L
LKS32MC057M6S8	96	32	2.5	6	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes							SSOP24L
LKS32MC057EM6S8	96	32	2.5	6	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~28		5V LDO	SSOP24L
LKS32MC057FM6S8	96	32	2.5	6	12BITx1	2	6	2	3 路	1	1	2		Yes	Yes		3P3N	+0.05/-0.3	7.5~28		5V LDO	SSOP24L

3 Pin Assignment

3.1 Pin Assignment and Pin Function Description

3.1.1 Special Notes

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.
SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32MC051C6T8

Fig. 3-1 LKS32MC051C6T8 Pin Assignment

3.1.3 LKS32MC052K6Q8

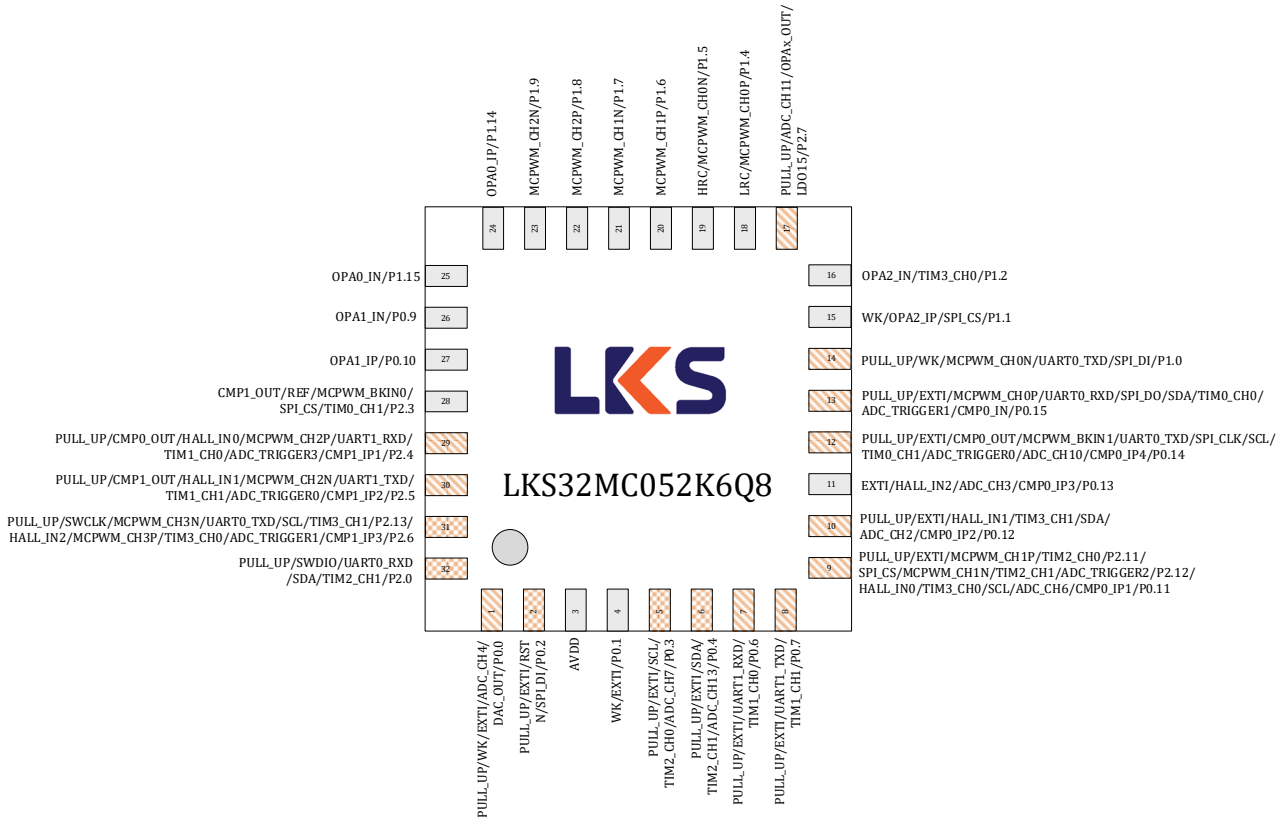

Fig. 3-2 LKS32MC052K6Q8 Pin Assignment

3.1.4 LKS32MC057M6S8

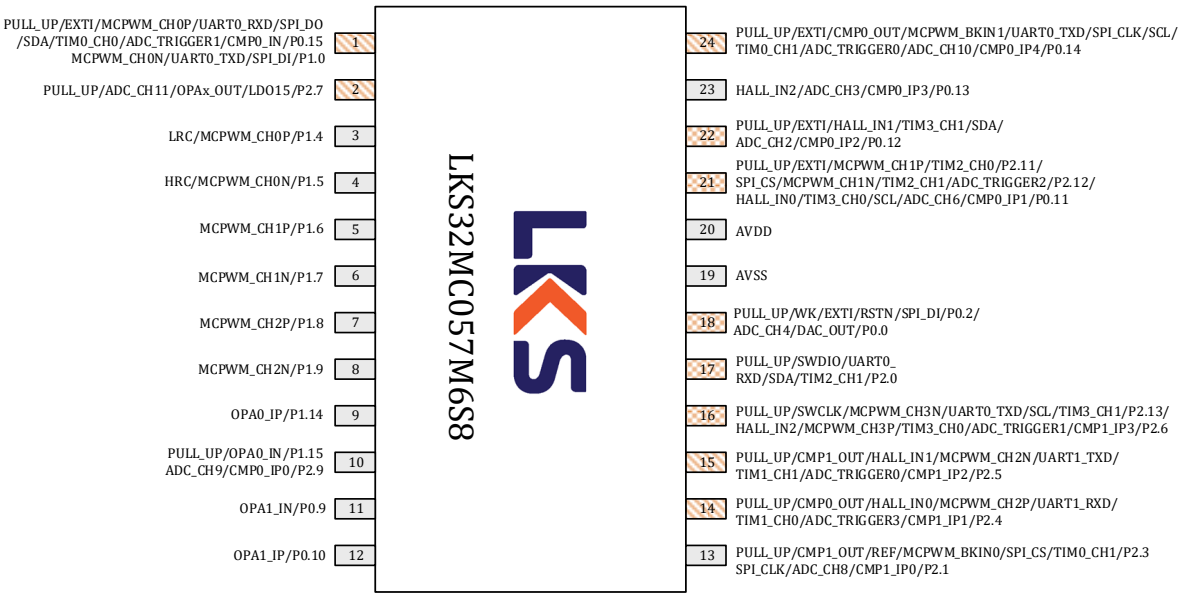

Fig. 3-3 LKS32MC057M6S8 Pin Assignment

* The red pin in the figure is the built-in pull-up resistor to AVDD:
100kΩ built-in pull-up resistor for RSTN, which is enabled automatically.
10kΩ built-in pull-up resistor for SWDIO/SWCLK, which is enabled automatically.
The remaining red pins are 10kΩ built-in pull-up resistors, which are software-enabled.

3.2 Pin Multiplex Function

Table 3-1 LKS32MC05x Pin Function Description

#	Pin			Pin name	Type	Function
	051	052	057			
1	1	1	18	PULL_UP/WK/EXTI/ADC_CH4/DAC_OUT/P0.0	IO	Pull up/Wake up/External interruption/ADC channel 4/DAC output/P0.0, built-in 10kΩ pull-up resister
2	2	2	18	PULL_UP/EXTI/RSTN/SPI_DI(DO)/P0.2	IO	Pull up/External interruption/RSTN/SPI data input(output)/P0.2, default as external reset，connected to a 100nF capacitor to ground, built-in 100kΩ pull-up resister
3	3	0	19	AVSS	GND	System ground
4	4	3	20	AVDD	PWR	Chip power supply, voltage range 2.2~5.5V。Decoupling capacitor should be larger than 1uF, and be places to AVDD pin as close as possible
5	5	4		WK/EXTI/P0.1	IO	Wake up/External interruption/P0.1
6	6	5		PULL_UP/EXTI/SCL/TIM2_CH0/ADC_CH7/P0.3	IO	Pull up/External interruption/IIC clock signal/Timer2 channel 0/ADC channel 7/P0.3, built-in controllable 10kΩ pull-up resister
7	7	6		PULL_UP/EXTI/SDA/TIM2_CH1/ADC_CH13/P0.4	IO	Pull up/External interruption/IIC data signal/Timer2 channel1/ADC channel 13/P0.4, built-in controllable 10kΩ pull-up resister
8	8			PULL_UP/EXTI/ADC_CH12/P0.5	IO	Pull up/External interruption/ADC channel 12/P0.5，built-in controllable 10kΩ pull-up resister
9	9	7		PULL_UP/EXTI/UART1_TX(RX)/TIM1_CH0/P0.6	IO	Pull up/External interruption/UART1 TX(RX)/Timer1 channel 0/P0.6，built-in controllable 10kΩ pull-up resister
10	10	8		PULL_UP/EXTI/UART1_TX(RX)/TIM1_CH1/P0.7	IO	Pull up/External interruption/UART1 TX(RX)/Timer1 channel 1/P0.7，built-in controllable 10kΩ pull-up resister
11	11	9	21	EXTI/MCPWM_CH1P/TIM2_CH0/P2.11	IO	External interruption/PWM channel 1 high side/Timer2 channel 0/P2.11
12	12	9	21	SPI_CS/MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	IO	SPI CS signal/PWM channel 1 low side/Timer2 channel 1/ADC trigger 2/P2.12
13	13	9	21	PULL_UP/EXTI/HALL_IN0/TIM3_CH0/ADC_CH6/CMP0_IP1/SCL/P0.11	IO	Pull up/External interruption/Hall sensor A-phase input/IIC clock/Timer3 channel 0/ADC channel 6/Comparator0 positive input channel 1/P0.11，built-in controllable 10kΩ pull-up resister
14	14	10	22	PULL_UP/EXTI/HALL_IN1/TIM3_CH1/ADC_CH2/CMP0_IP2/SDA/P0.12	IO	Pull up/External interruption/Hall sensor B-phase input/IIC data/Timer3 channel 1/ADC channel 2/Comparator0 positive input channel 2/P0.12，built-in controllable 10kΩ pull-up resister
15	15	11	23	EX-	IO	External interruption/Hall sensor C-phase input/ADC chan-

#	Pin			Pin name	Type	Function
	051	052	057			
				TI/HALL_IN2/ADC_CH3/CMP0_IP3/P0.13		nel 3/Comparator0 positive input channel 3/P0.13
16	16	12	24	PULL_UP/EXTI/CMP0_OUT/MCPWM_BKIN1/UART0_TX(RX)/SPI_CLK/SCL/TIM0_CH1/ADC_TRIG0/ADC_CH10/CMP0_IP4/P0.14	IO	Pull up/External interruption/Comparator0 output/PWM break input 1/UART0 TX(RX)/SPI Clock/IIC clock/Timer0 channel 1/ADC trigger 0/ ADC channel 10/Comparator0 positive input channel 4/P0.14，built-in controllable 10kΩ pull-up resister
17	17	13	1	PULL_UP/EXTI/MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/SDA/TIM0_CH0/ ADC_TRIG1/CMP0_IN/P0.15	IO	Pull up/External interruption/PWM channel 0 high side/UART0 TX(RX)/SPI data input(output)/IIC data/Timer0 channel 0/ADC trigger 1/ Comparator1 negative input /P0.15，built-in controllable 10kΩ pull-up resister
18	18	14		PULL_UP/WK/MCPWM_CH0N/ UART0_TX(RX)/SPI_DI(DO)/P1.0	IO	Pull up/Wake up/PWM channel 0 low side/UART0 TX(RX)/ SPI data input(output)/ P1.0，built-in controllable 10kΩ pull-up resister
19	19			PULL_UP/TIM3_CH1/ADC_CH5/P1.3	IO	Pull up/Timer3 channel 1/ADC channel 5/P1.3，built-in controllable 10kΩ pull-up resister
20	20	15		WK/OPA2_IP/SPI_CS/P1.1	IO	Wake up/OPA2 positive input /SPI_CS signal/P1.1
21	21	16		OPA2_IN/TIM3_CH0/P1.2	IO	OPA2 negative input /Timer3 channel 0/P1.2
22	22	17	2	PULL_UP/ADC_CH11/OPAx_OUT/LDO15/P2.7	IO	Pull up/ADC channel 11/OPAx output/LDO15 output/P2.7，built-in controllable 10kΩ pull-up resister
23	23			OPA3_IP/SPI_DI(DO)/SCL/P2.14	IO	OPA3 positive input /SPI_DI(DO) signal/IIC clock/P2.14
24	24			PULL_UP/OPA3_IN/SPI_CS/SDA/P2.15	IO	Pull up/OPA3 negative input /SPI_CS signal/IIC data/P2.15，built-in controllable 10kΩ pull-up resister
25	25			UART0_TX(RX)/SPI_DI(DO)/TIM2_CH0/ P2.8	IO	UART0 TX(RX)/ SPI_DI(DO) signal/Timer2 channel 0/ P2.8
26	26			SPI_CLK/TIM0_CH0/ P1.13	IO	SPI_CLK signal/Timer0 channel 0/ P1.13
27	27	18	3	LRC/MCPWM_CH0P/P1.4	IO	64KHz RC clock output/PWM channel 0 high side/P1.4
28	28	19	4	HRC/MCPWM_CH0N/P1.5	IO	4MHz RC clock output/PWM channel 0 low side/P1.5
29	29	20	5	MCPWM_CH1P/P1.6	IO	PWM channel 1 high side/P1.6
30	30	21	6	MCPWM_CH1N/P1.7	IO	PWM channel 1 low side/P1.7
31	31	22	7	MCPWM_CH2P/P1.8	IO	PWM channel 2 high side/P2.8
32	32	23	8	MCPWM_CH2N/P1.9	IO	PWM channel 2 low side/P1.9
33	33			MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0/ADC_TRIG2/P1.10	IO	PWM channel 3 high side/UART0 TX(RX)/IIC clock/Timer0 channel 0/ADC trigger 2/P1.10
34	34			PULL_UP/MCPWM_CH3N/UAR	IO	Pull up/PWM channel 3 low side/UART0 TX(RX)/IIC da-

#	Pin			Pin name	Type	Function
	051	052	057			
				T0_TX(RX)/SDA/TIM0_CH1/ADC_TRIG3/SIF/P1.11		ta/Timer0 channel 1/ADC trigger 3/P1.11，built-in controllable 10kΩ pull-up resister
35	35	24	9	OPA0_IP/P1.14	IO	OPA0 positive input /P1.14
36	36	25	10	OPA0_IN/P1.15	IO	OPA0 negative input /P1.15
37	37			PULL_UP/SPI_DI(DO)/SCL/ADC_CH9/CMP0_IP0/P2.9	IO	Pull up/SPI data input(output)/IIC clock/ADC channel 9/Comparator0 positive input channel 0/P2.9，built-in controllable 10kΩ pull-up resister
38	38			PULL_UP/SPI_DI(DO)/SDA/P2.10	IO	Pull up/SPI data input(output)/IICdata/P2.10，built-in controllable 10kΩ pull-up resister
39	39	26	11	OPA1_IN/P0.9	IO	OPA1 negative input /P0.9
40	40	27	12	OPA1_IP/P0.10	IO	OPA1 positive input /P0.10
41	41			PULL_UP/SPI_CLK/ADC_CH8/CMP1_IP0/P2.1	IO	Pull up/SPI clock/ADC channel 8/Comparator1 positive input channel 0/P2.1，built-in controllable 10kΩ pull-up resister
42	42			CMP1_IN/P2.2	IO	Comparator1 negative input /P2.2
43	43	28	13	CMP1_OUT/REF/MCPWM_BKIN0/SPI_CS/TIM0_CH1 /P2.3	IO	Comparator1 output/Voltage reference signal/PWM break input 0/SPI chip select signal/ P2.3
44	44	29	14	PULL_UP/CMP0_OUT/HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CMP1_IP1/P2.4	IO	Pull up/Comparator0 output/Hall sensor A-phase input/PWM channel 2 high side/UART1 TX(RX)/Timer1 channel 0/ADC trigger 3/Comparator1 positive input channel 1/P2.4，built-in controllable 10kΩ pull-up resister
45	45	30	15	PULL_UP/CMP1_OUT/HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/P2.5	IO	Pull up/Comparator1 output/Hall sensor B-phase input/PWM channel 2 low side/UART1 TX(RX)/Timer1 channel 1/ADC trigger 0/Comparator1 positive input channel 2/P2.5，built-in controllable 10kΩ pull-up resister
46	46	31	16	PULL_UP/HALL_IN2/MCPWM_CH3P/TIM3_CH0/ADC_TRIG1/CMP1_IP3/P2.6	IO	Pull up/Hall sensor C-phase input/PWM channel 3 high side /Timer3 channel 0/ADC trigger 1/Comparator1 positive input channel 3/P2.6，built-in controllable 10kΩ pull-up resister
47	47	31	16	PULL_UP/SWCLK/MCPWM_CH3N/UART0_TX(RX)/SCL/TIM3_CH1/P2.13	I	Pull up/SWD clock/PWM channel 3 low side/UART0 TX(RX)/IIC clock/Timer3 channel 1/P2.13，built-in uncontrollable 10kΩ pull-up resister
48	48	32	17	PULL_UP/SWDIO/UART0_TX(RX)/SDA/TIM2_CH1/P2.0	IO	Pull up/SWD data/UART0 TX(RX)/IIC data/Timer2 channel 1/P2.0，built-in uncontrollable 10kΩ pull-up resister

Table 3-2 LKS32MC05x Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFE	GPIO
P0.0										ADC_CH4, DAC_OUT	PULL_UP/WK/EXTI
P0.1											WK/EXTI
P0.2					SPI_DI(DO)						PULL_UP/EXTI
P0.3						SCL		TIM2_CH0		ADC_CH7	PULL_UP/EXTI
P0.4						SDA		TIM2_CH1		ADC_CH13	PULL_UP/EXTI
P0.5										ADC_CH12	PULL_UP/EXTI
P0.6				UART1_TX(RX)			TIM1_CH0				PULL_UP/EXTI
P0.7				UART1_TX(RX)			TIM1_CH1				PULL_UP/EXTI
P0.8											EXTI
P0.9										OPA1_IP	
P0.10										OPA1_IN	
P0.11		HALL_IN0				SCL		TIM3_CH0		ADC_CH6/CMP0_IP1	PULL_UP/EXTI
P0.12		HALL_IN1				SDA		TIM3_CH1		ADC_CH2/CMP0_IP2	PULL_UP/EXTI
P0.13		HALL_IN2								ADC_CH3/CMP0_IP3	EXTI
P0.14	CMP0_OUT		MCPWM_BKIN1	UART0_TX(RX)	SPI_CLK	SCL	TIM0_CH1		ADC_TRIG0	ADC_CH10/CMP0_IP4	PULL_UP/EXTI
P0.15			MCPWM_CH0P	UART0_TX(RX)	SPI_DI(DO)	SDA	TIM0_CH0		ADC_TRIG1	CMP0_IN	PULL_UP/EXTI

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFE	GPIO
P1.0			MCPWM_CH0N	UART0_TX(RX)	SPI_DI(DO)						PULL_UP/WK
P1.1					SPI_CS					OPA2_IP	WK
P1.2								TIM3_CH0		OPA2_IN	
P1.3								TIM3_CH1		ADC_CH5	
P1.4	LRC		MCPWM_CH0P								
P1.5	HRC		MCPWM_CH0N								
P1.6			MCPWM_CH1P								
P1.7			MCPWM_CH1N								
P1.8			MCPWM_CH2P								
P1.9			MCPWM_CH2N								
P1.10			MCPWM_CH3P	UART0_TX(RX)		SCL	TIM0_CH0		ADC_TRIG2		
P1.11			MCPWM_CH3N	UART0_TX(RX)		SDA	TIM0_CH1		ADC_TRIG3		PULL_UP
P1.12											
P1.13					SPI_CLK		TIM0_CH0				
P1.14										OPA0_IP	
P1.15										OPA0_IN	

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0	GPIO
P2.0				UART0_TX(RX)		SDA		TIM2_CH1			PULL_UP
P2.1					SPI_CLK					ADC_CH8/CMP1_IP0	PULL_UP
P2.2										CMP1_IN	
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			REF	
P2.4	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART1_TX(RX)			TIM1_CH0		ADC_TRIG3	CMP1_IP1	PULL_UP
P2.5	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART1_TX(RX)			TIM1_CH1		ADC_TRIG0	CMP1_IP2	PULL_UP
P2.6		HALL_IN2	MCPWM_CH3P					TIM3_CH0	ADC_TRIG1	CMP1_IP3	PULL_UP
P2.7										ADC_CH11/OPAx_OUT/LDO15	PULL_UP
P2.8				UART0_TX(RX)	SPI_DI(DO)			TIM2_CH0			
P2.9					SPI_DI(DO)	SCL				ADC_CH9/CMP0_IP0	PULL_UP
P2.10					SPI_DI(DO)	SDA					PULL_UP
P2.11			MCPWM_CH1P					TIM2_CH0			EXTI
P2.12			MCPWM_CH1N		SPI_CS			TIM2_CH1	ADC_TRIG2		
P2.13			MCPWM_CH3N	UART0_TX(RX)		SCL		TIM3_CH1			PULL_UP
P2.14					SPI_DI(DO)	SCL				OPA3_IP	
P2.15					SPI_CS	SDA				OPA3_IN	PULL_UP

4 Package Size

4.1 LKS32MC051C6T8

TQFP48 Profile Quad Flat Package:

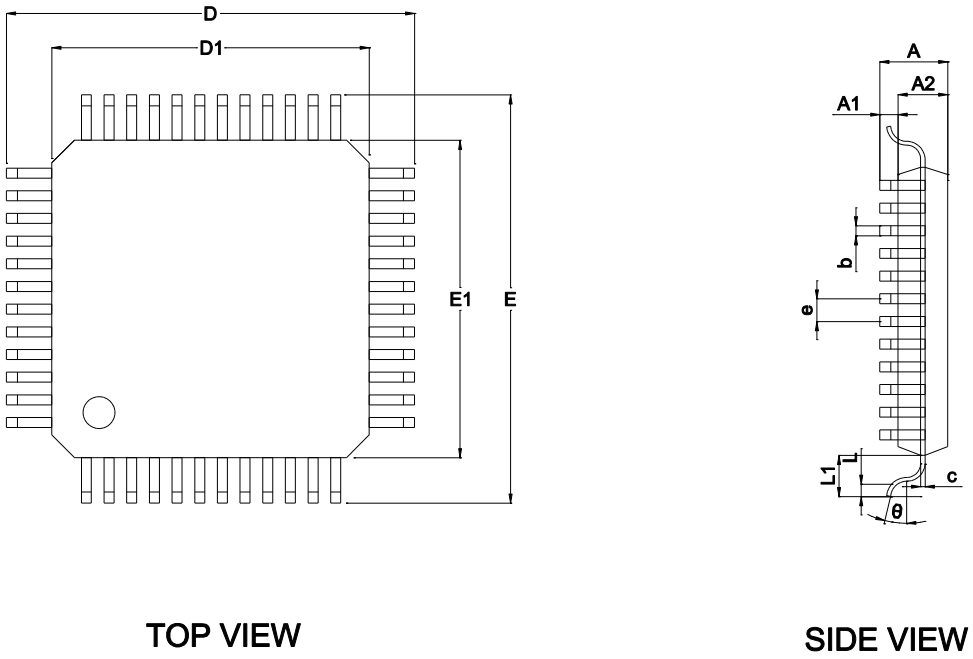

Fig. 4-1 LKS32MC051C6T8 Package Diagram

Table 4-1 LKS32MC051C6T8 Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.18	0.22	0.26
c	0.13	-	0.17
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	-	1.00	-

4.2 LKS32MC052K6Q8

QFN5*5 32L-0.75:

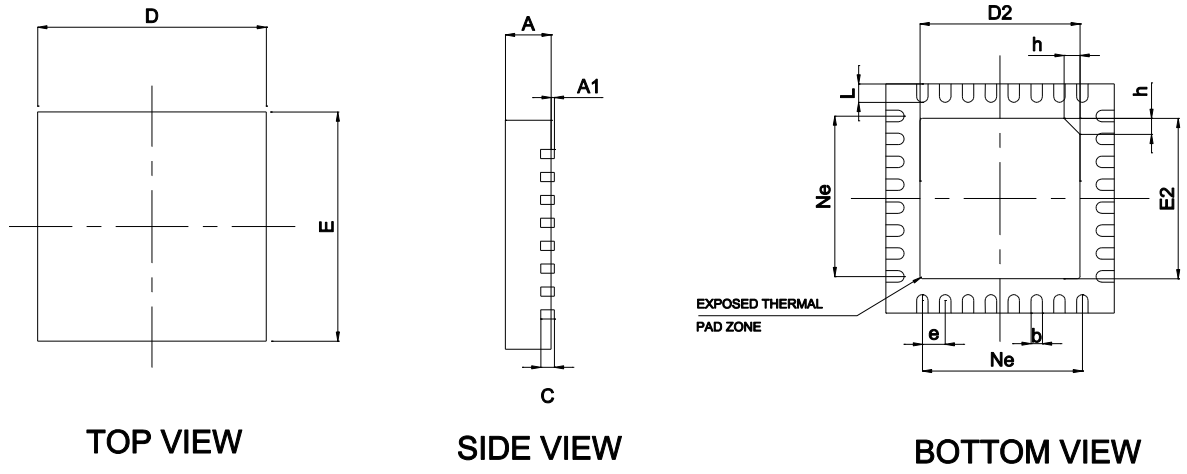

Fig. 4-2 LKS32MC052K6Q8 Package Diagram

Table 4-2 LKS32MC052K6Q8 Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.24
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

4.3 LKS32MC057M6S8

SSOP24L:

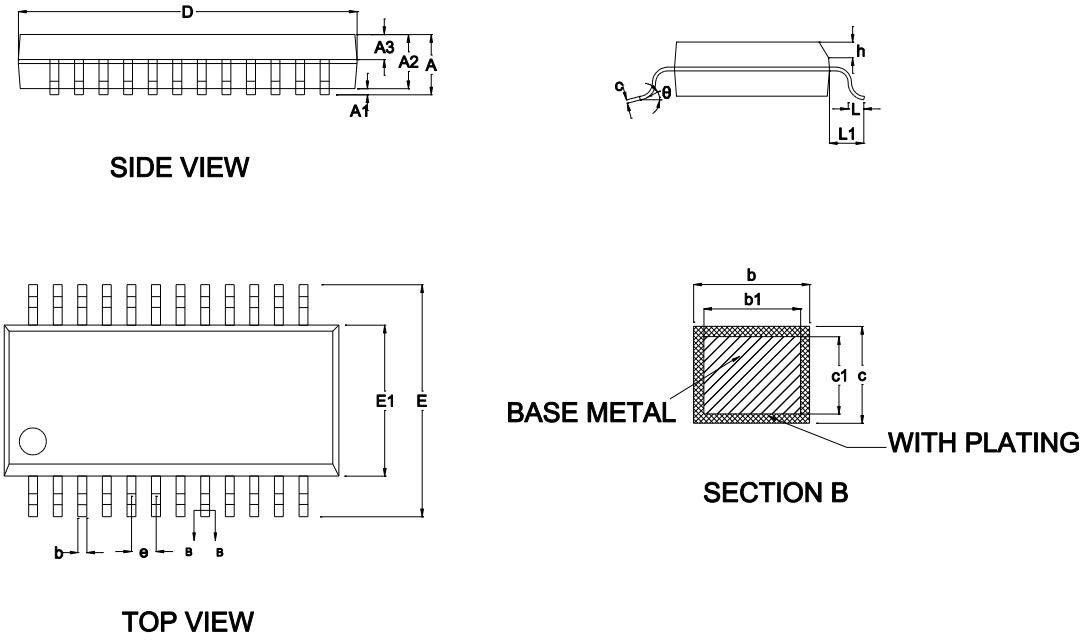

Fig. 4-3 LKS32MC057M6S8 Package Diagram

Table 4-3 LKS32MC057M6S8 Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

5 Electrical Characteristics

Table 5-1 LKS32MC05x Absolute Maximum Characteristics

Parameter	Min.	Max.	Unit	Description
Voltage (AVDD)	-0.3	+6.0	V	Ground
Operating Temperature	-40	+105	℃	
Storage Temperature	-40	+150	℃	
Junction Temperature	-	125	℃	
Pin Temperature	-	260	℃	solder for10 seconds

Table 5-2 LKS32MC05x Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Power Supply Voltage (AVDD)	2.2	5	5.5	V	
Analog Supply Voltage($AVDD_A$)	2.8	5	5.5	V	

OPA could work under 2.2V, but the output range will be limited.

Table 5-3 LKS32MC05x ESD parameters

Item	Min.	Max.	Unit
ESD test (HBM)	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC05x Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

Table 5-5 LKS32MC05x IO absolute characteristics

Parameter	Description	Min.	Max.	Unit
$V_{IN-GPIO}$	GPIO Signal Input Voltage Range	-0.3	6.0	V
I_{INJ_PAD}	Maximum Injection Current of a Single GPIO	-11.2	11.2	mA
I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 5-6 LKS32MC05x IO DC Parameters

Parameter	Description	AVDD	Conditions	Min.	Max.	Unit
V_{IH}	High input level of digital IO	5V	-	3.04		V
		3.3V		2.04		
V_{IL}	Low input level of digital IO	5V	-		0.3*AVDD	V
		3.3V			0.8	
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD		V
		3.3V				
I_{IH}	Digital IO current consumption when input is high	5V	-		1	uA
		3.3V				
I_{IL}	Digital IO current consumption when input is low	5V	-	-1		uA
		3.3V				
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8		V
V_{OL}	Low output level of digital IO		Current = 11.2mA		0.5	V
R_{pup}	Pull-up resistor*			8	12	kΩ
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit			100	200	Ω
C_{IN}	Digital IO Input-capacitance	5V	-		10	pF
		3.3V				

* Only some IOs have built-in pull-up resistors, see section “Pin Function Description” for details.

Table 5-7 LKS32MC05x Module Current/IDD

Module	Min	Typ	Max	Unit
CMP x1		0.005		mA
OPA x1		0.400		mA
ADC		1.510		mA
DAC		0.710		mA
Temp Sensor		0.150		mA
Band-Gap		0.154		mA
4MHz RC Clock		0.105		mA
PLL		0.080		mA
CPU+flash+SRAM (96MHz)		6.867		mA
CPU+flash+SRAM (12MHz)		1.300		mA
CRC		0.070		mA
UART		0.107		mA
MCPWM		0.053		mA
TIMER		0.269		mA
SPI		0.500		mA

IIC		0.500		mA
Sleep Mode	10	30	50	uA

The above tests, if not specifically marked, are all powered at room temperature 25° 5V, using 96MHz clock operating conditions, due to the manufacturing process there are device model deviations, the current consumption of different chips will have individual differences.

6 Power Management System

AVDD Power System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

AVDD is powered by a 2.2V ~ 5.5V supply, and all internal digital circuits and PLL modules are powered by an internal LDO15.

The LDO15 is automatically turned on after power-on. No software configuration is necessary. And the LDO15 output voltage can be adjusted by software.

The output voltage of LDO15 can be adjusted by setting register LDO15TRIM<2:0>. The corresponding value of the register can be seen in the analog register table. LDO15 has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again. If fine-tuning of the LDO output voltage is required, please read the original configuration value first, and then calculate the new settings accordingly.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.1V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation.

The PVD module monitors the 5V input power. If it is below a certain threshold, it will inform the MCU by sending an alarm (interrupt) signal.

7 Analog Characteristics

Table 7-1 LKS32MC05x analog characteristics

Parameter	Min.	Normal	Max.	Unit	Description
Analog-to-Digital Converter (ADC)					
Power Supply	2.8	5	5.5	V	
Sampling rate		3		MHz	$f_{adc}/16$
Differential Input Signal Range	-2.4 +0.048		+2.4 -0.048	V	When Gain=1;REF=2.4V
	-3.6 +0.072		+3.6 -0.072	V	When Gain=2/3;REF=2.4V
Single-ended Input Signal Range	-0.3		AVDD +0.3	V	Limited by the input voltage of the IO port
The differential signal is usually the signal output from the OPA inside the chip to the ADC; Single-ended signals are typically sampled externally via an I0 input: The ADC should measure the signal amplitude no more than ±98% of the full scale, regardless of the internal/external reference used. In particular, when using an external reference, it is recommended that the sampling conductor not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	500k			Ohm	
Input Capacitance		10pF		F	
Reference Voltage (REF)					
Power Supply	2.2	5	5.5	V	
Output Deviation	-9		9	mV	
Rejection Ratio of Power Supply		70		dB	
Temperature Coefficient		20		ppm/°C	
Output Voltage		1.2		V	
Digital-to-Analog Converter (DAC)					
Power Supply	2.2	5	5.5	V	
Load Resistance	5k			Ohm	Output BUFFER is on
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	

Parameter	Min.	Normal	Max.	Unit	Description
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational Amplifier (OPA)					
Power Supply	2.8	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load Resistance	20k			Ohm	
Load Capacitance			5p	F	
Input Common Mode Voltage Range (VICM)	0		AVDD	V	
Output Signal Range	0.1		AVDD-0.1	V	Under minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification xOFFSET
Common Mode Voltage (Vcm)	1.65	1.9	2.2	V	Measurement condition: normal temperature. Operational amplifier swing =2×min(AVDD-Vcm, Vcm). It is recommended to measure the Vcm and use software offset cancellation after powering on applications that use OPA single-end output. For more analysis, please refer to the official website application note ANN009-Differences between OPAmp Differential and Single-end Operating Modes.
Common Mode Rejection Ratio (CMRR)		80		dB	
Power Supply Rejection Ratio (PSRR)		80		dB	
Load Current			500	uA	
Slew Rate		5		V/us	
Phase Margin (PM)		60		Degree	
Comparator (CMP)					

Parameter	Min.	Normal	Max.	Unit	Description
Power Supply	2.2	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET		-19.2		mV	0 mV hysteresis, CMP output transitions from low to high
		-22.4		mV	0 mV hysteresis, CMP output transitions from high to low
		-18.4		mV	20 mV hysteresis, CMP output transitions from low to high
	-	8.1		mV	20 mV hysteresis, CMP output transitions from high to low
Delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'

Description of Analog Register Table:

Address space of 0x40000040 to 0x40000050 are the calibration registers of each analog module. These registers will be set to a unique calibration value in factory. Generally, users are advised not to configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x40000020 to 0x4000003c are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers could be configured in situations.

8 Clock System

The clock system consists of a 32KHz RC oscillator, a 4MHz RC oscillator, an external 4MHz crystal oscillator, and a PLL.

The 32K RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode; The 4MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz; The external 4MHz crystal oscillator is used as a backup clock.

Both 32k and 4M RC clocks will been through factory calibration, in the range of -40 ~ 105 ℃, the accuracy of the 32K RC clock is ± 50%, and the accuracy of the 4M RC clock is ± 1%.

The 4M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 4M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 4M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and could be enabled by software.

9 Reference Voltage

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = ’0’. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

The voltage reference can be measured by setting REF_AD_EN = ’1’ and via IO P2.3.

10 Analog Digital Converter

The chip integrated a SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 4M RC clock and PLL should be turned on first. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

ADC takes 16 ADC clock cycles to complete one conversion, of which 13 are conversion cycles and 3 are sampling cycles. I.E. $f_{conv}=f_{adc}/16$. When the ADC clock is set to 48MHz, the conversion rate is 3Msps.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, One-time 1 to 16 channels scanning mode, continuous 1 to 16 channels scanning mode. It has a set of 16 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

Among the 16 analog channels, the 19th channel is analog ground and is used to measure the offset of the ADC. The ADC values of other channels will be automatically subtracted by this offset. The offset is calibrated in factory and store in flash. Each time the chip is powered up, this offset will be loaded into ADC_DC register automatically. If the user needs to improve the offset over the whole temperature, it can be recalculated time by time (for example, each hour) when the ADC is idle.

When GAIN_REF = 0, the ADC voltage reference is 2.4V. The ADC has two gain modes, which are set by GAIN_SHAx, corresponding to 1x and 2/3 x gain setting; 1x gain corresponds to an input signal range of ± 2.4V, and 2/3 gain corresponds to an input signal range of ± 3.6V. When measuring the output signal of the OPA, select the specific ADC gain according to the maximum signal that the OPA may output.

11 Operational Amplifier

2-channel of rail-to-rail OPAs are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 4-channels amplifiers by setting OPAOUT_EN <2:0>, and send it to the P2.7 IO port through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description"). Because of this buffer, the OPA is able to be output to an IO while operating normally.

When the chip is powered on, the OPA module is OFF by default. It can be turned on by setting OPAxPDN = ’1’, and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 2-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay is 0.15uS. and the hysteresis voltage can be set to 20mV/0mV by CMP_HYS.

The signal sources of the positive and negative inputs can be programmed by register CMP_SELP<2:0> and CMP_SELN<1:0>. For details, please refer to the analog register description.

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

13 Temperature Sensor

The chip has a temperature sensor with an accuracy of ±2°C. The temperature sensor will be calibrated in factory, and the calibration value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = ’1’, and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 Digital Analog Converter

The chip has a 1-channel 12bit DAC, the maximum range of the output signal can be set to 1.2V/3V/4.85V through the register DAC_GAIN <1:0>.

The 12bit DAC can be output via IO port P0.0 by setting register DACOUT_EN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output data rate of the DAC is 1Msps.

When the chip is powered on, the DAC module is OFF by default. DAC can be turned on by setting DAC12BPDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor

- 32-bit Cortex-M0 + CORDIC/SQRT Co-processor
- Two-wire SWD debug pin
- System frequency is up to 96MHz

16 Memory

16.1 Flash

- Embedded flash including 32kB main area and 1kB NVR(Non-Volatile Register)
- Erase operation＞20,000 times
- Data retention duration is longer than 100 years at room temperature
- Single byte program takes 7.5us(max), Sector erase operation takes 5ms(max)
- Sector size 512bytes
- Support sector erase and program
- Support in-application program
- Flash data anti-theft(when the last word is programmed any word other than 0xFFFFFFFF)

16.2 SRAM

- Embedded 2.56kB SRAM

17 Motor Control PWM

- MCPWM operating frequency is up to 96MHz
- Supports up to 4 channels of complementary PWM output with adjustable phase
- The width of dead-zone in each channel can be configured independently
- Support edge-aligned PWM
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simutaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support capture mode for measuring external signal/pulse width
- Support comparison mode for timed interruption of edge-aligned PWM

19 Hall Sensor Interface

- Built-in 1024 cycles filtering
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 General Peripherals

- Two UART, full-duplex operation, support 7/8 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- Hardware watchdog, driven by RC clock and which is independent of system high-speed clock,the reset time ranges from 0.064s to 32s, the minimum step size is 0.064s.

21 Special IO Multiplexing

Notes for Special IO Multiplexing of LKS05x

The SWD protocol includes two signals: SWCLK and SWDIO. The former is a clock signal. To the chip, it is an input and will always be an input. The latter is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Users could use two IOs of SWD as GPIOs. The IO SWCLK could be multiplexed by P2.13, and the IO SWDIO could be multiplexed by P2.0. The precautions are as follows:

- The default state of multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[6] to enable multiplexing. I.e., after the hard reset of the chip, the initial state of IO s are SWD. Both IOs of SWD shall be provided with pull-up resistors inside the chip (the internal pull-up resistor of the chip is about 10K). When the IOs are used as SWD functions, the pull-up resistors are turned on by default and cannot be turned off. When IO is used as GPIO, the pull-up resistor can be controlled by GPIO2_PUE[13] and GPIO2_PUE[0]. P2.0 and P2.13 are forced to be used as SWD function within the 30ms after chip power-on reset. The software can write 1 to SYS_RST_CFG[6], but IO function switching won't take effect before 30ms after POR. The 30ms is counted by LRC. There is certain deviation due to the process reason.
- After multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. The greater margin means the greater probability of the successful one-time erasion.
- Secondly, the program should include a multiplexing exit mechanism. For example, a change in some other IO level (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In the packages of SSOP24L, QFN5*5 40L-0.75 and SOP16L, SWDIO may be directly bonded with P0.0, SWCLK may be directly bonded with P2.6. When P2.6 and SWCLK are bonded together, it is generally recommended to multiplex SWCLK as P2.13 to prevent SWCLK from always being in the input state, which will cause SWCLK to malfunction when the P2.6 signal changes.

If only SWCLK is multiplexed at this time, and SWDIO is not multiplexed, the precautions are the same as above.

For RSTN signal, the default is for the external reset pin of LKS05x chip.

LKS05x can realize the function of RSTN multiplexing as other IOs, and the multiplexed IO is P 0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

22 Ordering Information

Tray Package:

Package Type	Quantity per disc/tube	Quantity in box	Quantity in case
SOP16/ESOP16L	3000/ disc	6000PCS	48000PCS
SSOP24	4000/ disc	8000PCS	64000PCS
SS0P24	50/ pipe	10000PCS	4000/100000PCS
QFN 8*8	260/ disc	2600PCS	15600PCS
QFN 4*4/5*5/6*6	490/ disc	4900PCS	29400PCS
QFN 3*3	5000/ disc	5000PCS	40000PCS
LQFP48/TQFP48 0707	250/ disc	2500PCS	15000PCS
LQFP64 1010	160/ disc	1600PCS	9600PCS
LQFP100 1414	90/ disc	900PCS	5400PCS
TSSOP20/28	4000/ disc	8000PCS	64000PCS

Reel Package:

Package Type		Quantity per disc/tube	Quantity per box	Quantity boxes per case	Quantity per case
Braid -13 inches	SOP/ESOP8	4000	8000	8	64000
Braid -13 inches	SOP/ESOP16	3000	6000	8	48000
Braid -13 inches	SSOP24	4000	8000	8	64000
Braid -13 inches	TSSOP20	4000	8000	8	64000
Braid -13 inches	D/QFN3*3	5000	10000	8	80000
Braid -13 inches	D/QFN4*4	5000	10000	8	80000
Braid -13 inches	D/QFN5*5	5000	10000	8	80000
Pipe	SOP16	50	10000	10	100000
Pipe	SOP14/SSOP24	50	10000	10	100000
Pipe	TSSOP24	54	6480	6	38880

23 Version History

Table 23-1 Document's Version History

Date	Version No.	Description
2025.08.22	1.79	Update naming rules
2025.07.21	1.78	Delete the Flash section: While one Sector is erased and written, another Sector can be read and accessed at the same time.
2024.08.04	1.77	Order package information updates to confirm package information by package type and package form
2023.09.25	1.76	Update welding temperature
2023.04.07	1.75	Update package description
2023.03.22	1.74	Modify the LSI precision range
2023.03.02	1.73	change Vcm 1.65~2.2
2023.01.14	1.72	Add ordering information
2022.11.10	1.71	Add connection resistance between IO and internal analog circuit, change Vcm 1.7~2.2
2022.06.11	1.7	Modified some parameters of GPIO
2021.02.06	1.6	057 Added the P1.0 sleep wake interface
2021.02.01	1.5	057 pin 10/13 added functionality
2020.12.30	1.4	Modify the RSTN pin description
2021.01.29	1.3	Update DSP description
2020.03.19	1.2	Modify some pin definitions
2019.07.18	1.1	Revise 051's definition
2019.03.10	1.0	Initial version

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