Linko Semiconductor Co., Ltd.
南京凌鸥创芯电子有限公司

LKS32MC03x with built-in 6N Gate Driver

32bit Compact MCU for Motor Control

Features

○ 48MHz 32-bit Cortex-M0 core, hardware division coprocessor
○ 30uA low-power sleep mode, MCU sleep power consumption is 30uA
○ -40-105℃ industrial-grade operating temperature range
○ MCU uses 2.5V~5.5V single power supply
○ Super antistatic and anti-group pulse capability

Storage

○ Three specifications including 16kB flash/16kB flash+16kB ROM/32kB flash, with a flash anti-stealing feature
○ 4kB RAM

Timer

○ Built-in 4MHz high-precision RC timer, with a full temperature range accuracy of ±1%
○ Built-in64kHz low-speed timer for use in low-power mode
○ Internal PLL providing up to a 48MHz timer

Peripherals

○ One UART
○ One SPI
○ One IIC
○ General-purpose 16-/32-bit timer, supporting capture and edge-aligned PWM
○ Dedicated PWM module for motor control, supporting 6 PWM outputs, independent dead zone control
○ Dedicated interface for Hall signals, supporting speed measurement and debounce
○ 4-channel DMA
○ Hardware watchdog
○ Supports up to 25 GPIOs

Analog Module

○ Integrated one 12-bit SAR ADC, 1Msps sampling and conversion rate, 11 channels in total
○ Integrated 2 OPA, settable for a differential PGA mode
○ Integrated two comparators
○ Integrated 8-bit DAC digital-to-analog converter as an internal comparator input
○ Built-in 1.2V voltage reference with an accuracy of 0.5%
○ Built-in 1 low-power LDO and power monitoring circuit
○ Integrated high-precision, low-temperature drift high-frequency RC timer

Key Strengths

✧ The internal integration of 2 high-speed operational amplifiers can meet the different requirements of single-resistor/dual-resistance current sampling topology;
✧ The input port of the operational amplifier integrates a voltage clamp protection circuit, and only two external current-limiting resistors are needed to achieve direct current sampling of the MOSFET internal resistance;
✧ ADC module variable gain technology can work with high-speed operational amplifiers to handle a wider dynamic range of current and take into account the sampling accuracy of small current and large current;
✧ Integrated two-way comparator;
✧ Strong ESD and anti-interference ability, stable and reliable;
✧ supply to ensure the versatility of system power supply.
✧ Supports IEC/UL60730 functional safety certification

Application Scenarios

Applicable to control systems such as BLDC/ Sensorless BLDC/ FOC/Sensorless FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, digital power source etc.

1 Overview

1.1 Function Description

The LKS32MC03x_6N series are 32-bit core compact MCU intended for motor control applications that integrates all the modules required for common motor control systems. The MCU integrates three-phase full-bridge bootstrapping gate drive modules, which can directly drive six N-type MOSFETs.

- **Performance**
  - 48MHz 32-bit Cortex-M0 core
  - Low-power sleep mode
  - Integrated three-phase full-bridge bootstrapping gate drive modules
  - Industrial-grade operating temperature range
  - Super antistatic and anti-group pulse capability
- **Memory**
  - 32 kB Flash with encryption, a 128-bit chip unique identifier
  - 4kB RAM
  - Operating temperature: -40~105℃
- **Timer**
  - Built-in 4MHz high-precision RC timer, with an accuracy within ±1% in a range of -40~105℃
  - Built-in 64kHz low-speed timer for use in low-power mode
  - Internal PLL providing up to a 48MHz timer
- **Peripheral Module**
  - One UART
  - One SPI for master-slave mode
  - One IIC for master-slave mode
  - One general-purpose 16-bit timer, supporting capture and edge-aligned PWM functions
  - One general-purpose 32-bit timer, supporting capture and edge-aligned PWM functions;
  - Dedicated PWM module for motor control, supporting 8 PWM outputs, independent dead zone control
  - Dedicated interface for Hall signals, supporting speed measurement and debounce functions
  - Hardware watchdog
  - 25 GPIOs. Eight GPIOs can be used as wake-up sources for the system. 17 GPIOs can be used as external interrupt source inputs
- **Analog Module**

- Integrated one 12-bit SAR ADC, 1.2Msps sampling and conversion rate, 11 channels in total
- Integrated a 2-channel operational amplifier, settable for a differential PGA mode
- Integrated two comparators
- Integrated 8-bit DAC digital-to-analog converter
- Built-in ±2°C temperature sensor
- Built-in 1.2V voltage reference with an accuracy of 0.5%
- Built-in 1 low-power LDO and power monitoring circuit
- Integrated high-precision, low-temperature drift high-frequency RC timer

1.2 Key Strengths

- High reliability, high integration, small volume of final product, saving BOM costs.
- Internally integrated 2-channel high-speed operational amplifier and two comparators to meet the different requirements of single-resistor/dual-resistor current sampling topologies;
- Internal high-speed operational amplifier integrating high-voltage protection circuits, allowing the high-level common-mode signal to be directly input into the chip, and realizing the direct current sampling mode of MOSFET resistance with the simplest circuit topology;
- The application of patented technology enables the ADC and high-speed operational amplifier to match best, which can handle a wider current dynamic range, while taking into account the sampling accuracy of high-speed small current and low-speed large current;
- The overall control circuit is simple and efficient, with stronger anti-interference ability, more stable and reliable;
- Integrated three-phase full-bridge bootstrapping gate drive modules;
- LKS32MC031KLC6T8B/LKS32MC034DOF6Q8/LKS32MC034SF6Q8 with an integrated 5V LDO internally

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, etc.;

1.3 Naming Conventions

LKS32 MC 037 M 6 S 8 (X)

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

031KL	= 1 ADC, 2 PGA, 6N Driver, 5V LDO
033	= 1 ADC, 2 PGA
034D	= 1 ADC, 2 PGA, 6N Driver
034DO	= 1 ADC, 2 PGA, 6N Driver, 5V LDO
034S	= 1 ADC, 2 PGA, 6N Driver, 5V LDO, DBOOT
035D,035E	= 1 ADC, 1 PGA, 3P3N Driver, 5V LDO
033,037,038	= 1 ADC, 2 PGA
037E,037F,039	= 1 ADC, 2 PGA, 3P3N Driver, 5V LDO
039PL5	= 1 ADC, 2 PGA, MOS, 5V LDO
039PL3	= 1 ADC, 2 PGA, MOS, 3.3V LDO

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
Y	= 28 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory
D	=384Kbyte Flash Memory
E	=512Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Version

X	= Version, B~Z

Figure 1-1 LKS32MC03x Device Naming Conventions

1.4 System Resources

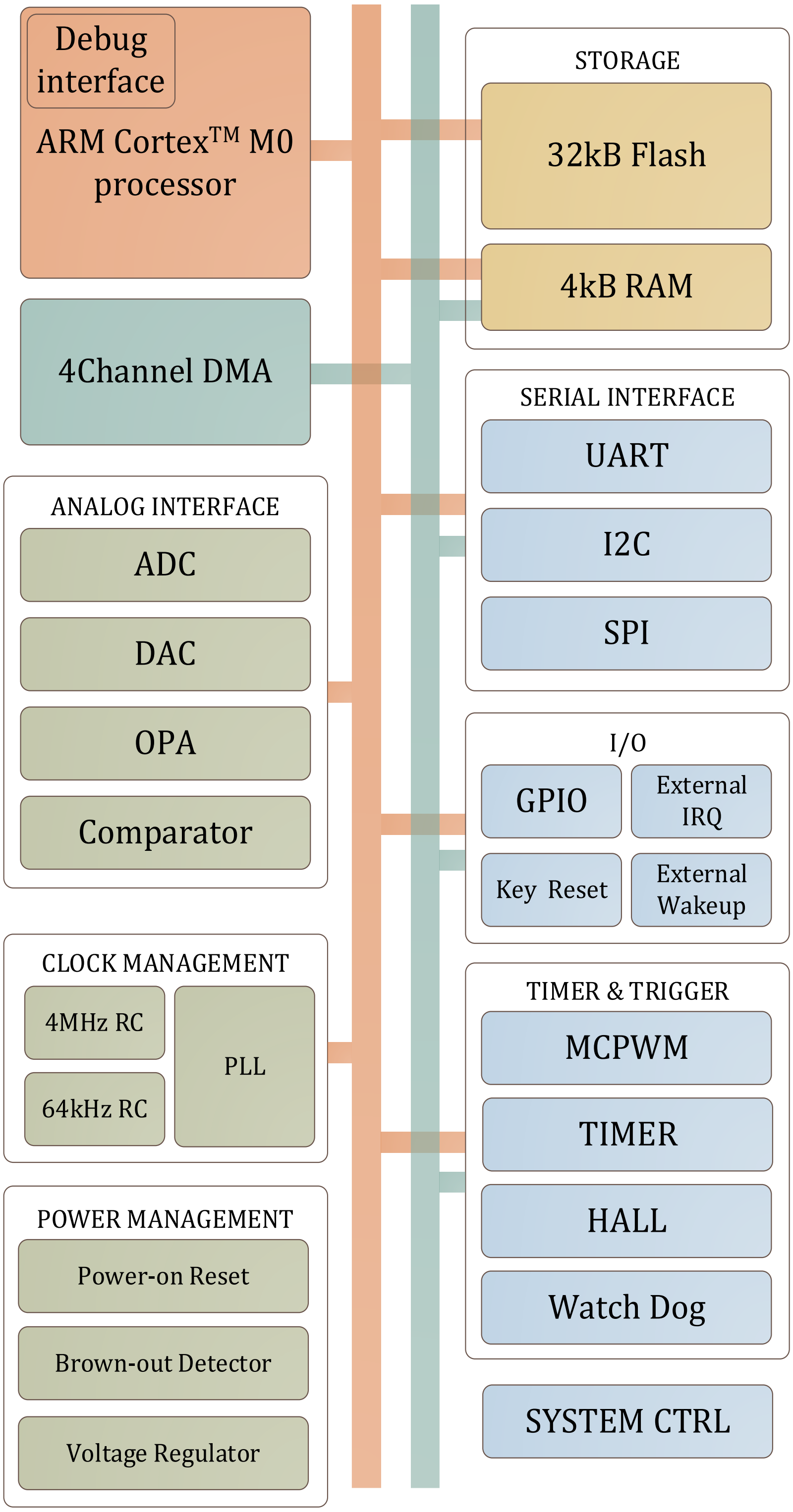

Figure 1-2 LKS32MC03x System Block Diagram

1.5 FOC System

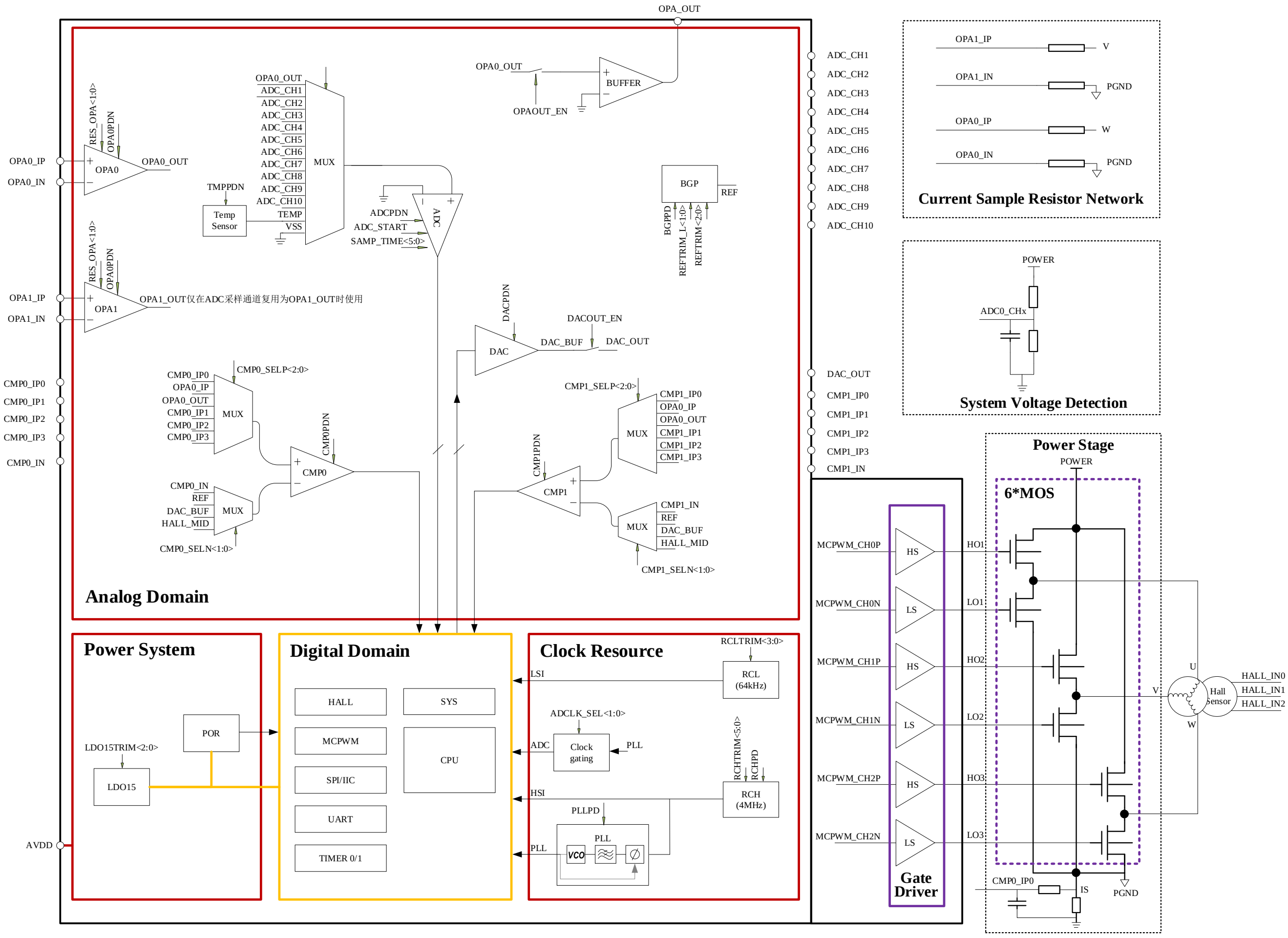

Figure 1-3 Simplified Schematic Diagram of the LKS32MC03x Vector Sinusoidal Control System

2 Device Selection Table

Table 2-1 LKS03x Series Device Selection Table

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	Temp. Sensor	PLL	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC031KLC6T8B	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+0.2/-0.35	13-20	600	5V LDO	LQFP48L 0707
LKS32MC031KLC6T8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+0.2/-0.35	13-20	600	5V LDO	LQFP48L 0707
LKS32MC031PC6Q8C*	48	32	4	9	8BITx1	2	6	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	DFN5.0*6.0 48L
LKS32MC032LK6T8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes						LQFP32
LKS32MC033H6P8	48	32	4	7	8BITx1	2	5	1	3	1	1	1	Yes	Yes						TSSOP20L
LKS32MC033H6P8B	48	32	4	7	8BITx1	2	5	2	3	1	1	1	Yes	Yes						TSSOP20L
LKS32MC033H6P8C	48	32	4	7	8BITx1	2	5	2	3	1	1	1	Yes	Yes						TSSOP20L
LKS32MC033H6Q8	48	32	4	7	8BITx1	2	5	1	3	1	1	1	Yes	Yes						QFN3*3 20L-0.75
LKS32MC033H6Q8B	48	32	4	7	8BITx1	2	5	1	3	1	1	1	Yes	Yes						QFN3*3 20L-0.75
LKS32MC033H6Q8C	48	32	4	7	8BITx1	2	5	1	3	1	1	1	Yes	Yes						QFN3*3 20L-0.75
LKS32MC034DF6Q8	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	7-20	200		QFN5*5 40L-0.75
LKS32MC034DF6Q8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	7-20	200		QFN5*5 40L-0.75
LKS32MC034DF6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	7-20	200		QFN5*5 40L-0.75
LKS32MC034DOF6Q8	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	7-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034DOF6Q8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	7-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034DOF6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	7-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034SF6Q8	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034SF6Q8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75

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LKS32MC034SF6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034S2F6Q8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034S2F6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034FLF6Q8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034FLF6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN5*5 40L-0.75
LKS32MC034FLK6Q8C	48	32	4	7	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN4*4 32L-0.75
LKS32MC034F2LF6Q8C	48	32	4	8	8BITx1	2	7	2	3	0	1	1	Yes	Yes	6N	+1/-1	-0.3-48	90	5V LDO	QFN5*5 40L-0.75
LKS32MC034F2LM6Q8C	48	32	4	5	8BITx1	2	3	2	2	0	1	1	Yes	Yes	6N	+1/-1	-0.3-48	90	5V LDO	QFN4*4 24L-0.75
LKS32MC034FLNK6Q8C	48	32	4	5	8BITx1	2							Yes	Yes	6N	+1/-1.2	4.5-20	200	5V LDO	QFN4*4 32L-0.75
LKS32MC034F2LNK6Q8C	48	32	4	5	8BITx1	2	4	2	3	0	1	1	Yes	Yes	6N	+1/-1	-0.3-48	90	5V LDO	QFN4*4 32L-0.75
LKS32MC0342FLK6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes	6N	+1/-1	-0.3-48	200	5V LDO	QFN4*4 32L-0.75
LKS32MC035DL6S8	48	32	4	6	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16L
LKS32MC035DL6S8B	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16L
LKS32MC035DL6S8C	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16L
LKS32MC035EL6S8B	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SOP16L
LKS32MC035EL6S8C	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SOP16L
LKS32MC037M6S8	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes						SSOP24L
LKS32MC037M6S8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes						SSOP24L
LKS32MC037M6S8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes						SSOP24L
LKS32MC037EM6S8	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24L
LKS32MC037EM6S8B	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24L
LKS32MC037EM6S8C	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24L
LKS32MC037FM6S8B	48	32	4	8	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SSOP24L
LKS32MC037FM6S8C	48	32	4	8	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SSOP24L
LKS32MC037LM6S8B	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	SSOP24L
LKS32MC037LM6S8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	SSOP24L

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LKS32MC037QM6Q8	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 24L-0.75
LKS32MC037QM6Q8B	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 24L-0.75
LKS32MC037QM6Q8C	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 24L-0.75
LKS32MC037Q2M6Q8C	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	QFN4*4 24L-0.75
LKS32MC038Y6P8	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes						TSSOP28L
LKS32MC038Y6P8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes						TSSOP28L
LKS32MC038Y6P8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes						TSSOP28L
LKS32MC038LY6P8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	TSSOP28L
LKS32MC038LY6P8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	TSSOP28L
LKS32MC038LY6Q8B	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	QFN4x4 28L-0.75
LKS32MC038LY6Q8C	48	32	4	10	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	QFN4x4 28L-0.75
LKS32MC039DK6Q8B	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 32L-0.75
LKS32MC039DK6Q8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 32L-0.75
LKS32MC039PL5K6Q8B*	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	QFN5*5 32L-0.75
LKS32MC039PL5K6Q8C*	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	QFN5*5 32L-0.75
LKS32MC039PL3K6Q8B	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					3.3V LDO	QFN4*4 32L-0.75
LKS32MC039PL3K6Q8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					3.3V LDO	QFN4*4 32L-0.75

* LKS32MC039PL5K6Q8/LKS32MC039PL3K6Q8/LKS32MC031PC6Q8C integrate a three-phase full bridge circuit composed of three pairs of MOS.

3 Pin Assignment

3.1 Pin Assignment Diagram

3.1.1 Special Notes

PU is short for pull-up. The PU pin in the following pin diagrams is designed with an internal pull-up resistor to the AVDD.

The RSTN pin is equipped with an internal 100kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the RSTN function is switched to the GPIO function

The SWDIO/SWCLK comes with an internal 10kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the SWD function is switched to the GPIO function

The remaining PU pins have an internal 10kΩ pull-up resistor that can be turned on or off by software control.

EXTI is external interrupt or GPIO interrupt input pin.

WK is short for wake-up, is external wake-up source.

UARTx_TX(RX): UART supports an interchange between the TX and RX. When the second function of GPIO is selected as UART and GPIO_PIE i.e. input is enabled, it can be used as UART_RX; When GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

SPI_DI(DO): The DI and DO of SPI can be interchanged. When the second function of GPIO is SPI, and GPIO_PIE i.e. input is enabled, it can be used as SPI_DI; when GPIO_POE i.e. output is enabled, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 Version Difference

There are two versions for each package. The major difference is the pin location of ADC_CH6/ ADC_CH7. For details, please refer to the table below.

C version is recommended for new design.

Table 3-1 Version Comparison

<table>
<tr><th colspan="2">A Version</th><th colspan="2">B/C Version</th></tr>
<tr><td colspan="2">DAC output range 0~3V</td><td colspan="2">B Version: DAC output range0~3V/4.8V
C Version: DAC output range0~1.2V/3V/4.8V</td></tr>
<tr><td rowspan="3">P0_9</td><td>CLKO</td><td rowspan="3">P0_9</td><td>CLKO</td></tr>
<tr><td>MCPWM_CH0P</td><td>MCPWM_CH0P</td></tr>
<tr><td>UART0_RXD</td><td>UART0_RXD</td></tr>
</table>

	SPI_DO		SPI_DO
	SDA		SDA
	TIM0_CH1		TIM0_CH1
	ADC_TRIGGER		ADC_TRIGGER
	CMP0_IN		CMP0_IN
	PU		PU
	EXTI7		EXTI7
			ADC_CH6
	WK3		WK3
P0_10	CLKO	P0_10	CLKO
	MCPWM_CH0P		MCPWM_CH0P
	TIM0_CH0		TIM0_CH0
	TIM1_CH0		TIM1_CH0
	ADC_CH6		
	WK4		WK4
P0_15	MCPWM_CH2N	P0_15	MCPWM_CH2N
	TIM1_CH0		TIM1_CH0
	ADC_CH7		
	EXTI9		EXTI9
P1_6	CMP1_OUT	P1_6	CMP1_OUT
	HALL_IN1		HALL_IN1
	MCPWM_CH2N		MCPWM_CH2N
	UART0_TXD		UART0_TXD
	TIM0_CH1		TIM0_CH1
	ADC_TRIGGER		ADC_TRIGGER
			ADC_CH7
	CMP1_IP2		CMP1_IP2
	PU		PU
	EXTI12		EXTI12
P1_5	SPI_DI	P1_5	SPI_DI
	SCL		SCL
	TIM1_CH1		TIM1_CH1
	OPA1_IN		OPA1_IN
			ADC_CH8
	CMP1_IP0		CMP1_IP0
	PU		PU
	EXTI11		EXTI11
	WK5		WK5

In A Version, the chip doesn’t have ADC_CH8 pin. In B Version, users who don’t need OPA1, could use ADC_CH8 by setting SYS_OPA_SEL=0.

The chip contains an 8 bit DAC with an output signal range of 3 V for version A, 3 V/4.8 V for version B, and 1.2 V/3 V/4.8 V for version C.C chip, the SYS_AFE_REG2.BIT15 = 1 needs to be set to use the 1.2 V scale of the DAC.

By reading SYS_ AFE_ INFO.Version can view the chip version. 1 represents version A ,2 represents version B and 3 represents version C.

3.1.3 LKS32MC031KLC6T8B/ LKS32MC031KLC6T8C

Figure 3-1 LKS32MC031KLC6T8B(C) Pin Assignment Diagram

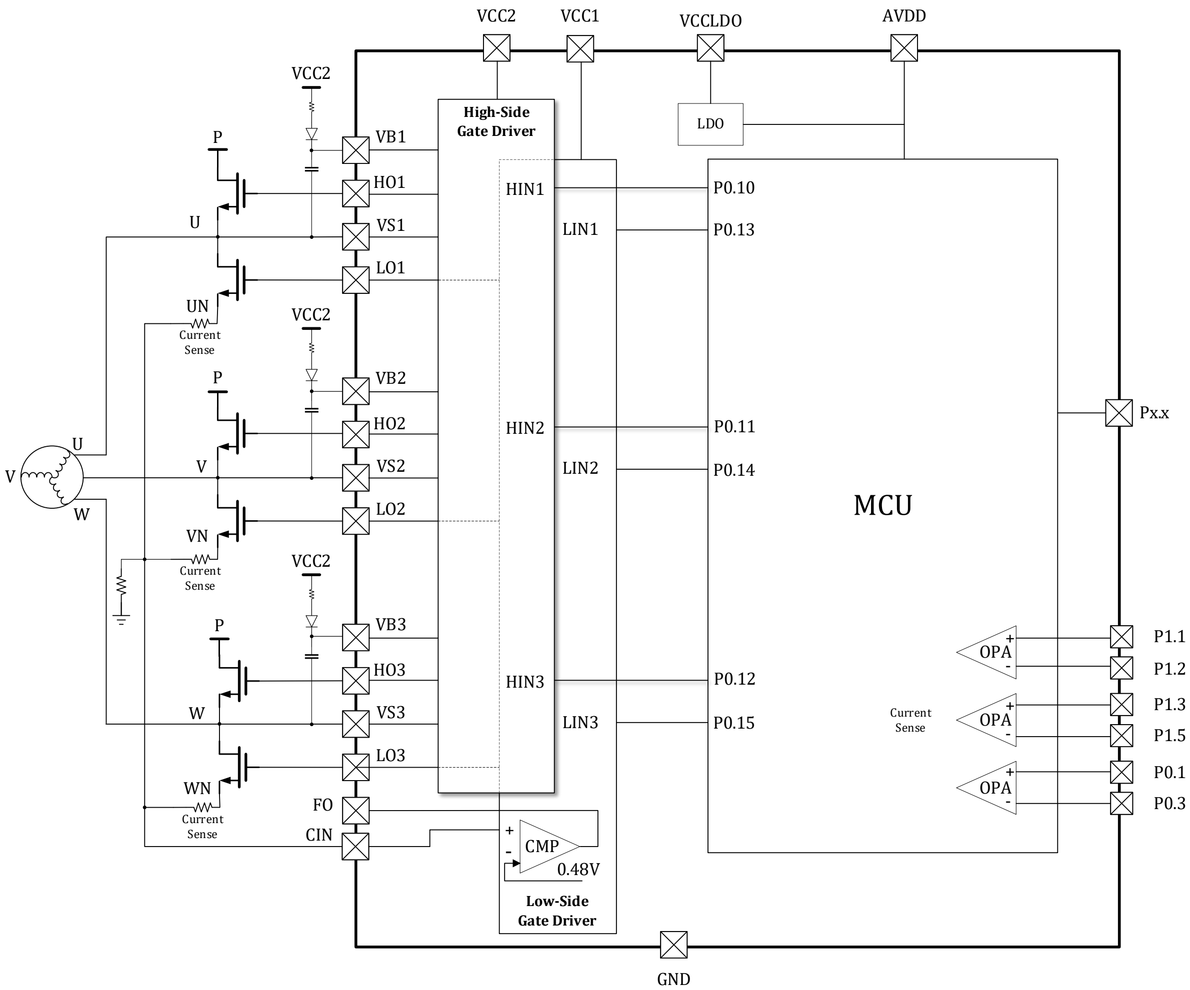

Figure 3-2 Schematic diagram of the LKS32MC031KLC6T8B(C) gate driver connection

Table 3-2 LKS32MC031KLC6T8B(C)Pin Description

1	VS1	High-side floating bias voltage 1.
2	HO1	Phase A high-side output, worked by MCU P0.10; the polarity of HO1 is the same as that of P0.10, i.e. when P0.10 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1. And exchange the P and N channel outputs of CH0 by setting MCPWM_ IO01.CH0_ PN_ SW=1。
3	VB1	High-side floating supply voltage 1.
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	GND	Ground
8	CIN	Current sense input. The MCU provides an over-current detection function by connecting the CIN input with the motor current feedback. The CIN comparator threshold (typ. 0.48V) is referenced to AGND ground. An input noise filter (typ. 250ns) prevents the driver to detect false over-current events. Over current detection generates a hard shutdown of all LO outputs of the gate driver and provides a latched fault feedback at Fo pin. The blocking time after over-current is fixed internally by 65us.

9	Fo	Fault feedback. Fo pin is an active low open-drain output indicating the status of the gate driver. The pin is active (i.e. force slow voltage level) when one of the following conditions occur: (1) Under-voltage condition of VCC supply; (2) Over-current detection (CIN). The fault detection signal will go to internal logic block which will disable LO outputs.
10	VCC1	Gate driver power supply 1, 13~20V. The pin is not connected to the gate drive power supply 2 inside the chip, and these two pins need to be powered separately.
11	LO1	Phase A low-side output, worked by MCU P0.13; the polarity of LO1 is the same as that of P0.13, i.e. when P0.13 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1. And exchange the P and N channel outputs of CH0 by setting MCPWM_ IO01.CH0_ PN_ SW=1。
12	LO2	Phase B low-side output, worked by MCU P0.14; the polarity of LO2 is the same as that of P0.14, i.e. when P0.14 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1. And exchange the P and N channel outputs of CH0 by setting MCPWM_ IO01.CH1_ PN_ SW=1。
13	LO3	Phase C low-side output, worked by MCU P0.15; the polarity of LO3 is the same as that of P0.15, i.e. when P0.15 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1. And exchange the P and N channel outputs of CH0 by setting MCPWM_ IO23.CH2_ PN_ SW=1。
14	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
15	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
16	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
17	P1_2	P1.2
	OPA0_IN	OPA0 negative input

18	P1_1	P1.1
	OPA0_IP	OPA0 positive input
19	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
20	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
21	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
22	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
23	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
24	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
25	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
26	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
27	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data

	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
28	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
29	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
30	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
31	GND	Ground
32	AVDD	5V LDO voltage output
33	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
34	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug

	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
35	VCC2	Gate driver power supply 2, 13~20V. The pin is not connected to the gate drive power supply 1 inside the chip, and these two pins need to be powered separately.
36	NC	Not connected
37	NC	Not connected
38	VB3	High-side floating supply voltage 3.
39	VS3	High-side floating bias voltage 3.
40	HO3	Phase C high-side output, worked by MCU P0.12; the polarity of HO3 is the same as that of P0.12, i.e. when P0.12 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1. And exchange the P and N channel outputs of CH0 by setting MCPWM_ IO23.CH2_ PN_ SW=1。
41	NC	Not connected
42	NC	Not connected
43	NC	Not connected
44	VS2	High-side floating bias voltage 2.
45	HO2	Phase B high-side output, worked by MCU P0.11; the polarity of HO2 is the same as that of P0.11, i.e. when P0.11 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1. And exchange the P and N channel outputs of CH0 by setting MCPWM_ IO01.CH1_ PN_ SW=1。
46	VB2	High-side floating supply voltage 2.
47	NC	Not connected
48	NC	Not connected

3.1.4 LKS32MC034DF6Q8

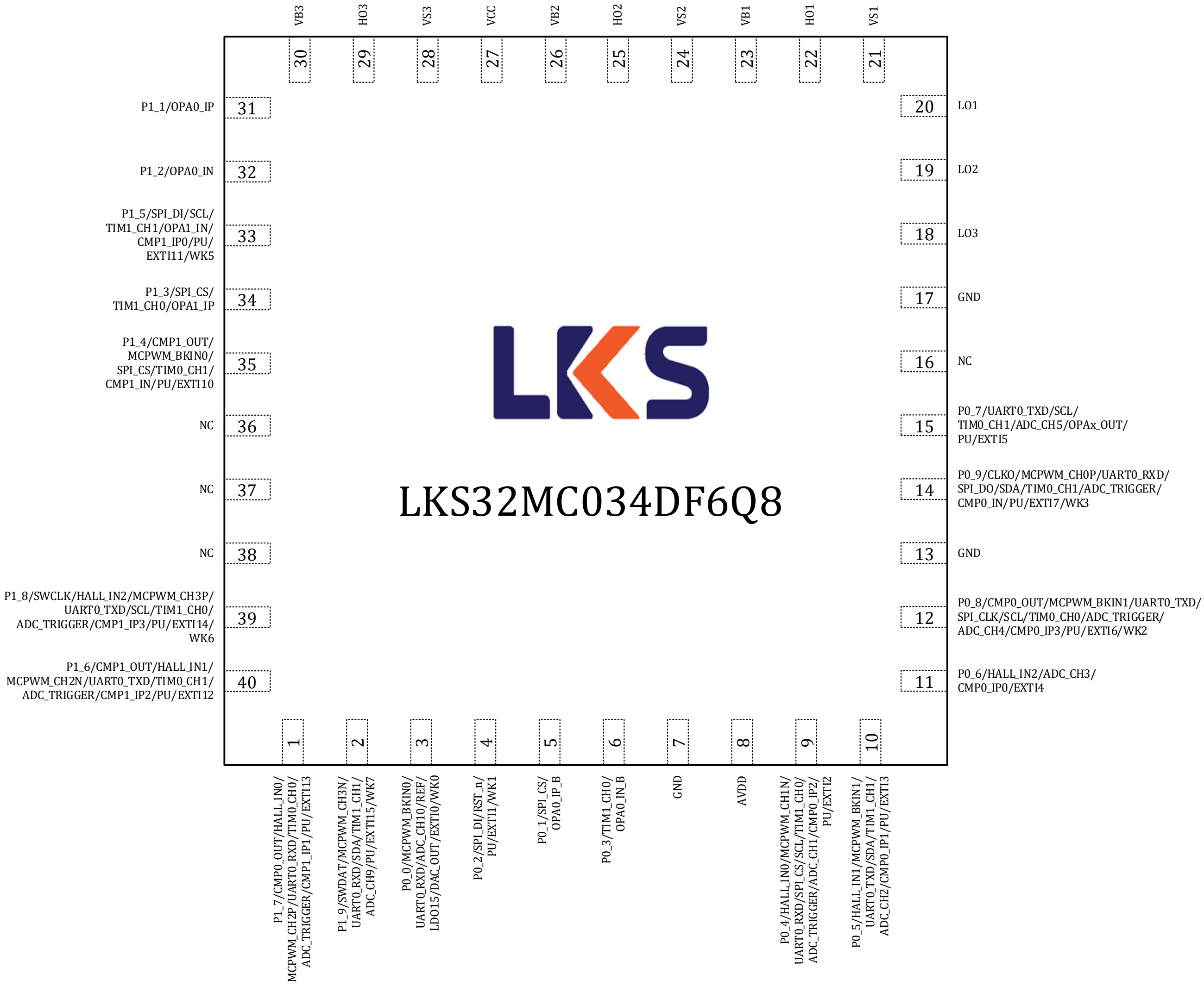

Figure 3-3 LKS32MC034DF6Q8 Pin Assignment Diagram

LKS32MC03x with built-in 6N Gate Driver

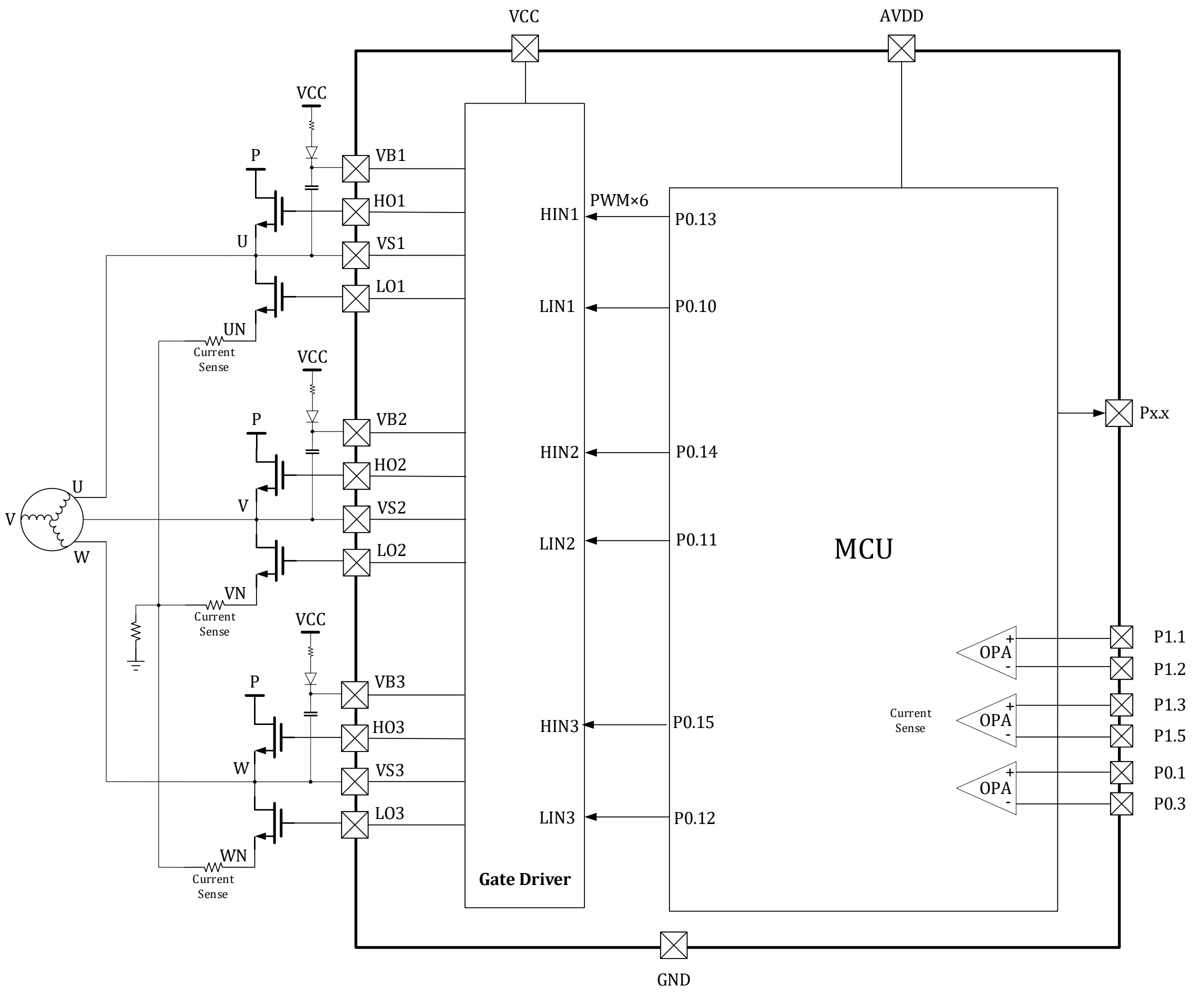

Figure 3-4 Schematic diagram of the LKS32MC034DF6Q8 gate driver connection

Table 3-3 LKS32MC034DF6Q8 Pin Description

0	GND	Chip ground, located on the belly of the chip
1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data

	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	Power supply, 2.5~5.5V
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2

10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)

	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	NC	Not connected
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0

	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.5 LKS32MC034DF6Q8B/ LKS32MC034DF6Q8C

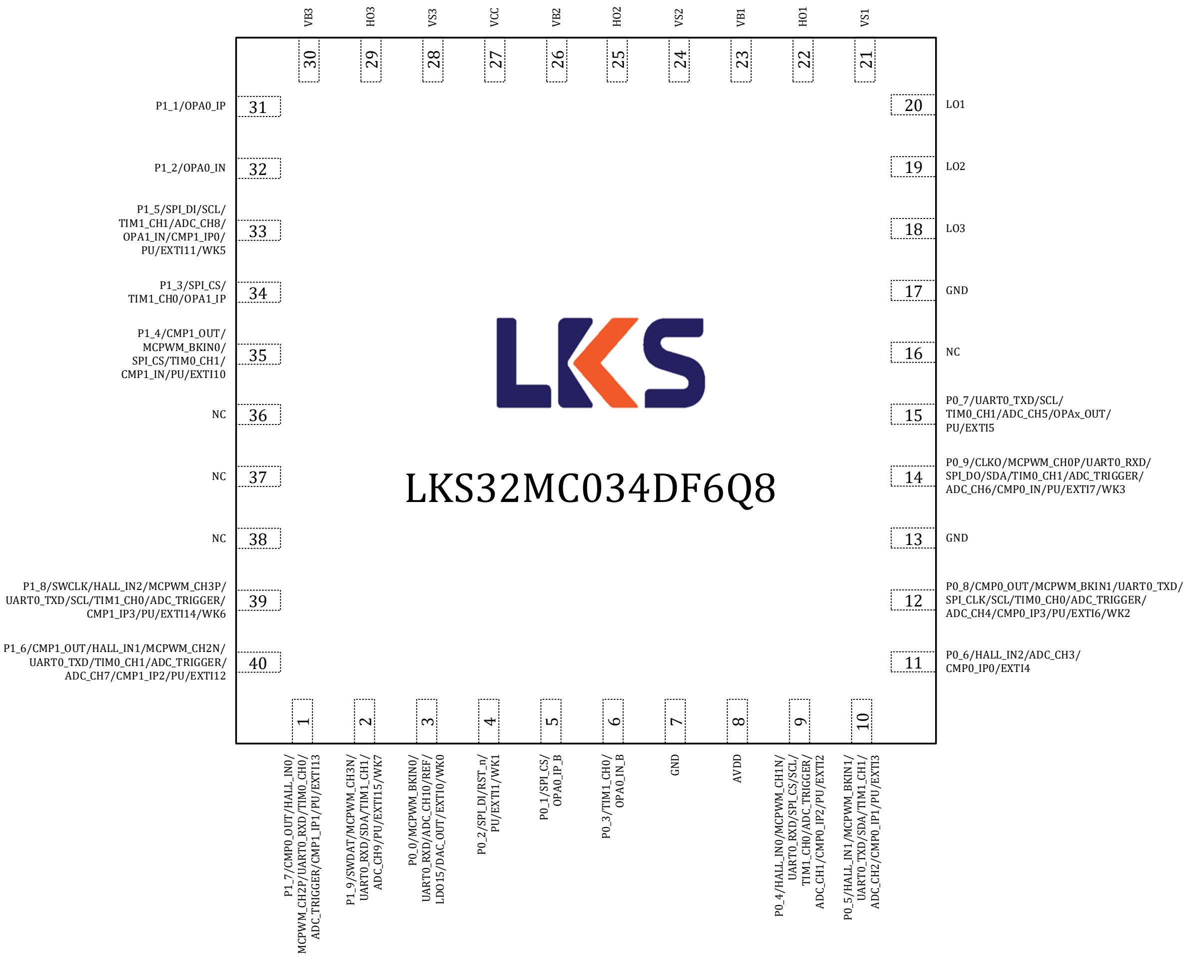

Figure 3-5 LKS32MC034DF6Q8B(C) Pin Assignment Diagram

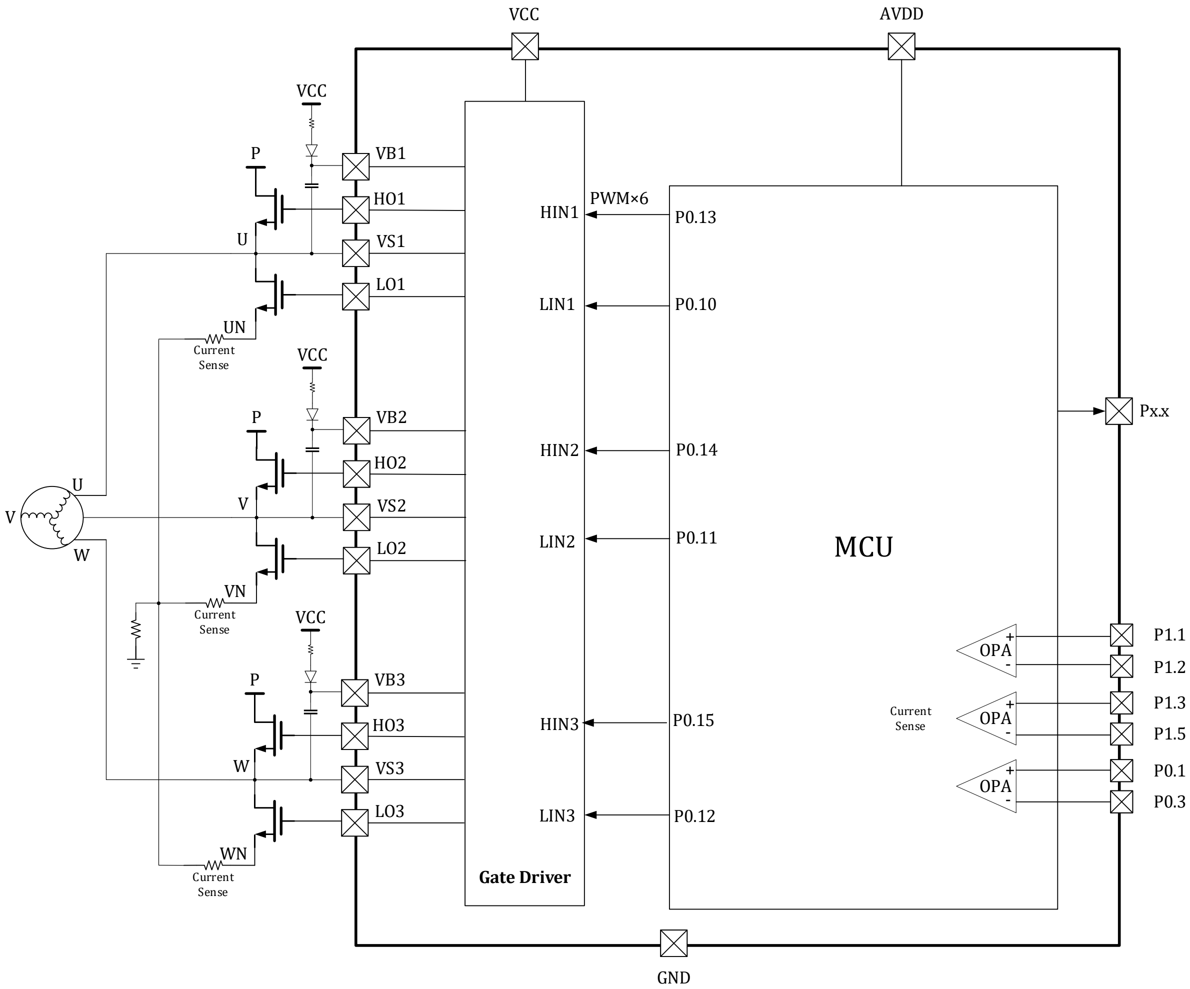

Figure 3-6 Schematic diagram of the LKS32MC034DF6Q8B(C) gate driver connection

Table 3-4 LKS32MC034DF6Q8B(C) Pin Description

0	GND	Chip ground, located on the belly of the chip
1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data

	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	Power supply, 2.5~5.5V
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2

10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7

	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	NC	Not connected
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3

	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.6 LKS32MC034DOF6Q8/LKS32MC034SF6Q8

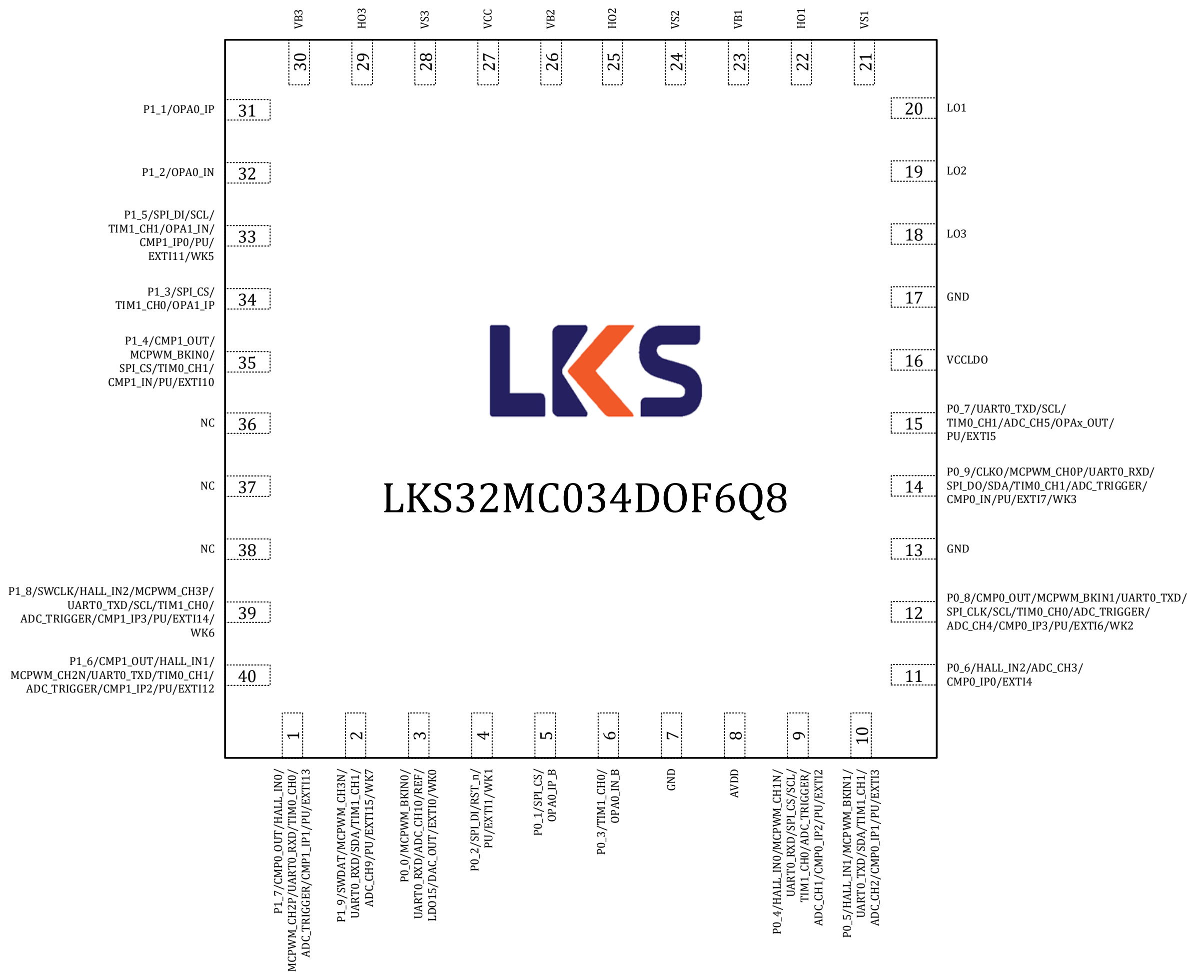

Figure 3-2 LKS32MC034DOF6Q8/LKS32MC034SF6Q8 Pin Assignment Diagram

The LKS32MC034DOF6Q8 is pin compatible with the LKS32MC034SF6Q8, which integrates a bootstrap diode between VCC and three-phase VBS.

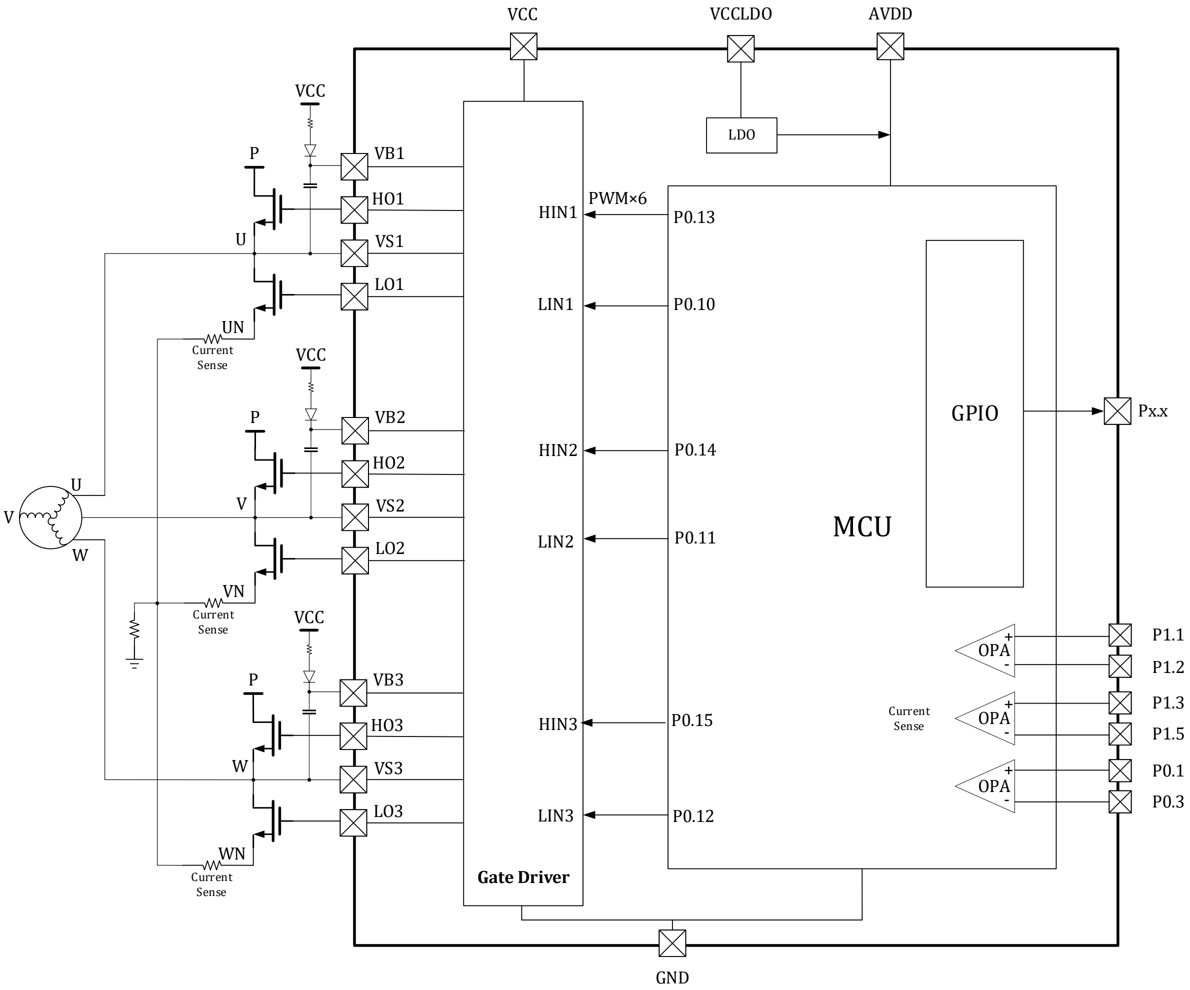

Figure 3-2 Schematic diagram of the LKS32MC034DOF6Q8/LKS32MC034SF6Q8 gate driver connection

Table 3-5 LKS32MC034DOF6Q8/LKS32MC034SF6Q8 Pin Description

0	GND	Chip ground, located on the belly of the chip
1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)

	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	5V LDO voltage output
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7

	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3

	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.7 LKS32MC034DOF6Q8B(C)/LKS32MC034SF6Q8B(C)

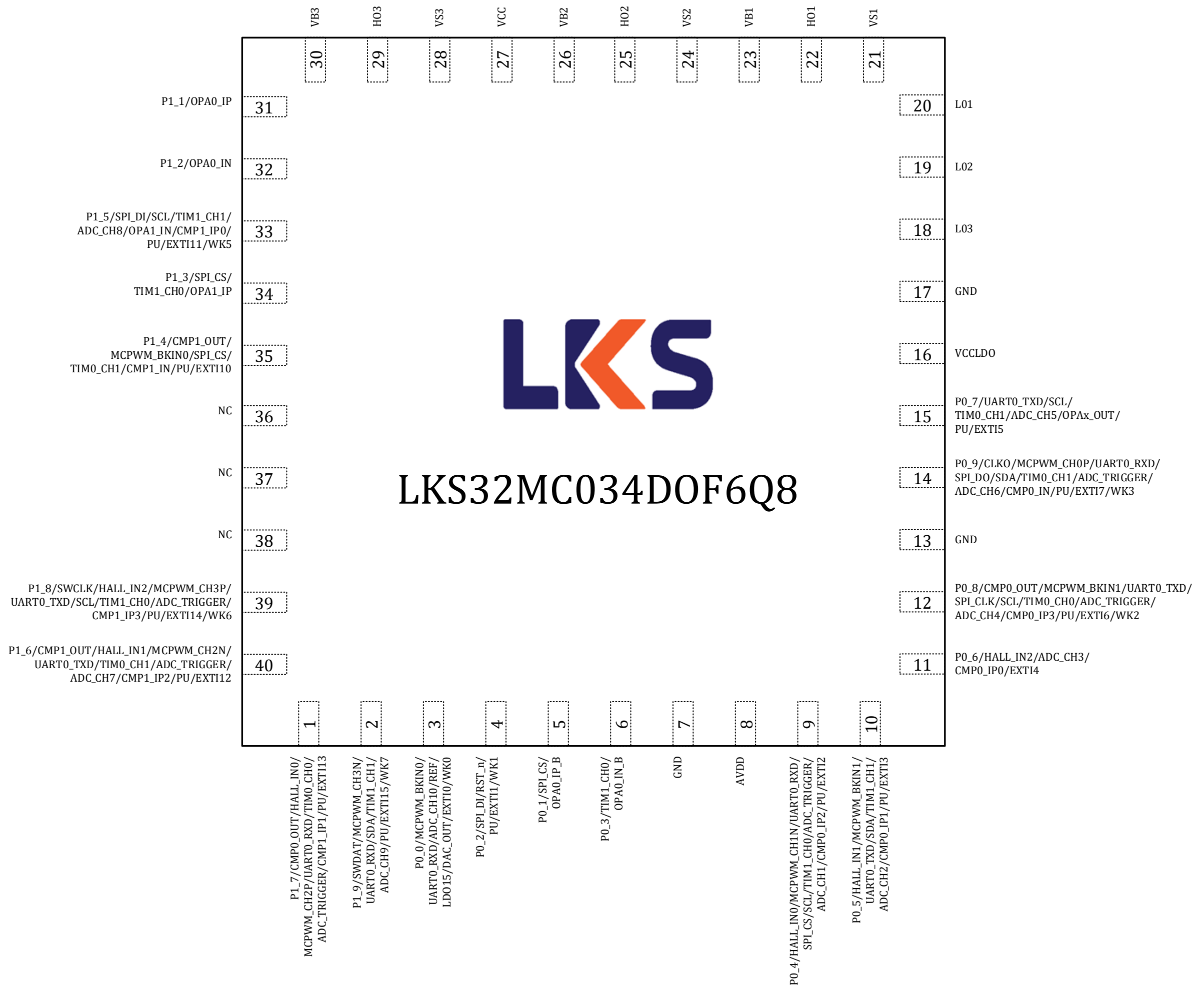

Figure 3-3 LKS32MC034DOF6Q8B(C)/LKS32MC034SF6Q8B(C) Pin Assignment Diagram

The LKS32MC034DOF6Q8 is pin compatible with the LKS32MC034SF6Q8, which integrates a bootstrap diode between VCC and three-phase VBS.

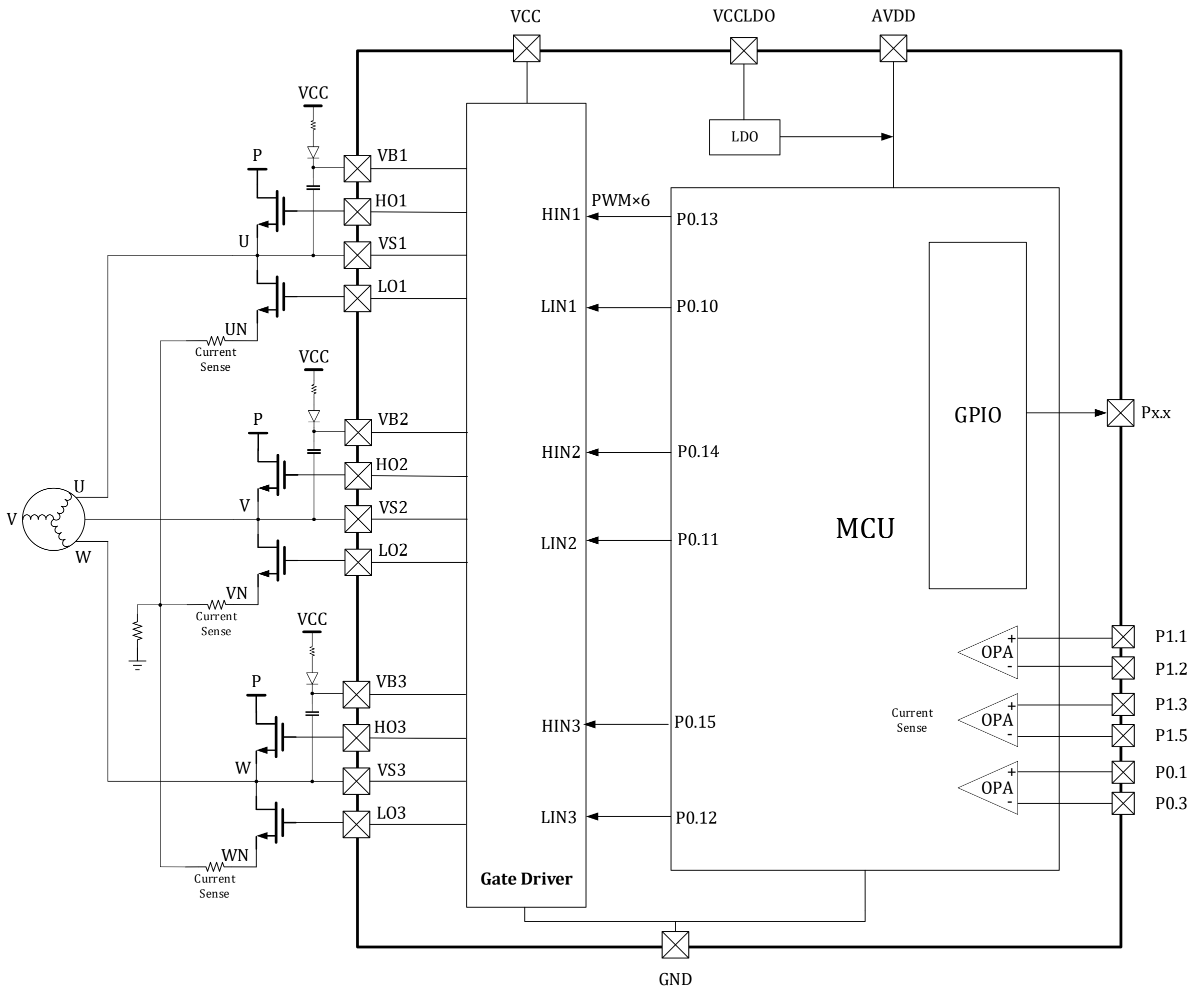

Figure 3-2 Schematic diagram of the LKS32MC034DOF6Q8B(C)/LKS32MC034SF6Q8B(C) gate driver connection

Table 3-6 LKS32MC034DOF6Q8B(C)/LKS32MC034SF6Q8B(C) Pin Description

0	GND	Chip ground, located on the belly of the chip
1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data

	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	5V LDO voltage output
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1

	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1

	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI12	External GPIO interrupt input signal 12

3.1.8 LKS32MC034S2F6Q8B/ LKS32MC034S2F6Q8C

Figure 3-6 LKS32MC034S2F6Q8B(C) Assignment Diagram

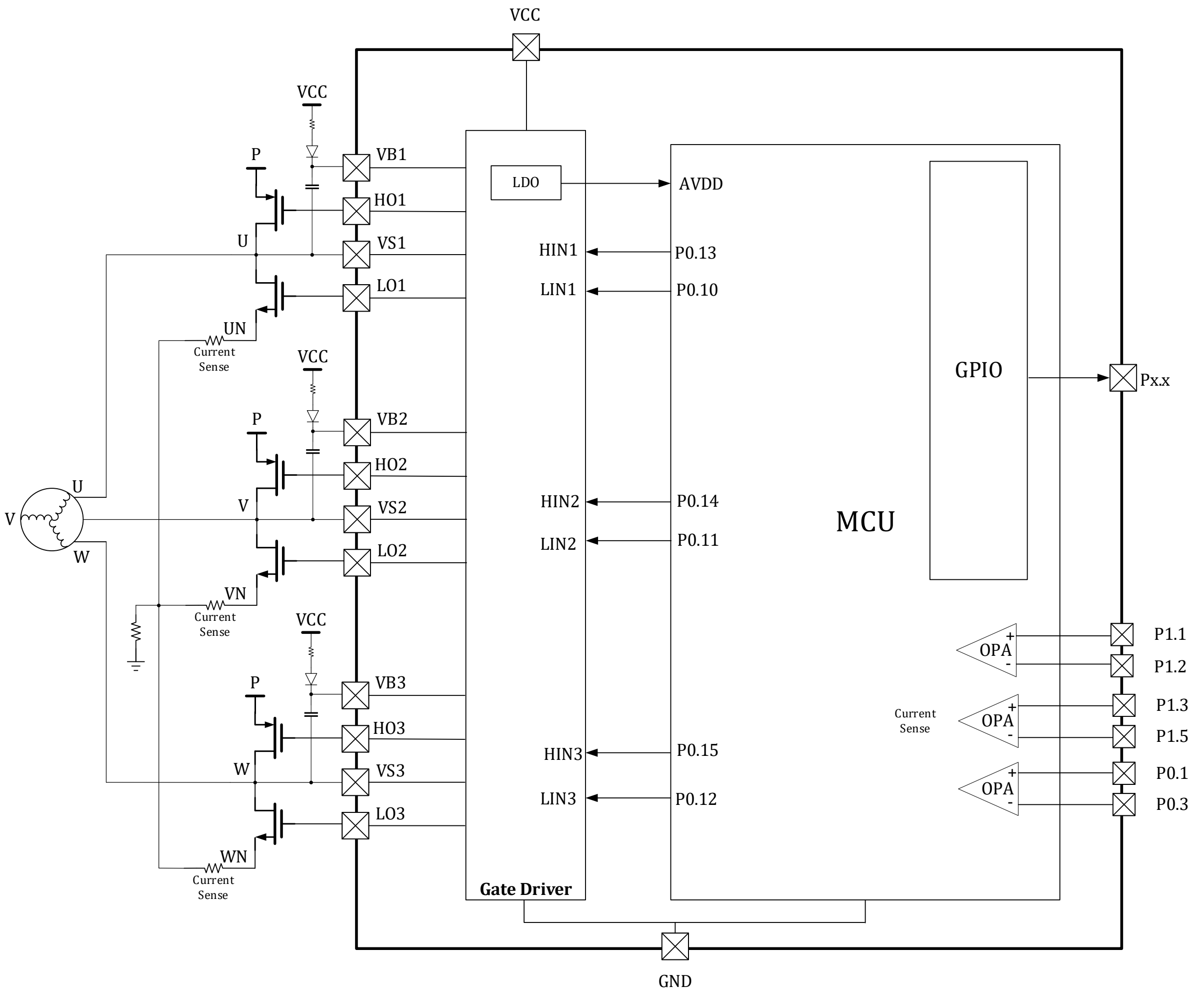

Figure 3-2 Schematic diagram of the LKS32MC034S2F6Q8B(C) gate driver connection

Table 3-7 LKS32MC034S2F6Q8B(C)Pin Description

1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1

	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	Power supply, 2.2~5.5V
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5

	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)

	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	NC	Not connected
17	GND	Ground
18	LO3	Phase A low-side output, worked by MCU P0.12; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase C low-side output, worked by MCU P0.10; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 3.
22	HO1	Phase C high-side output, worked by MCU P0.13; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 3.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply
28	VS3	High-side floating bias voltage 1.
29	HO3	Phase A high-side output, worked by MCU P0.15; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 1.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select

	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.9 LKS32MC034FLF6Q8B/ LKS32MC034FLF6Q8C

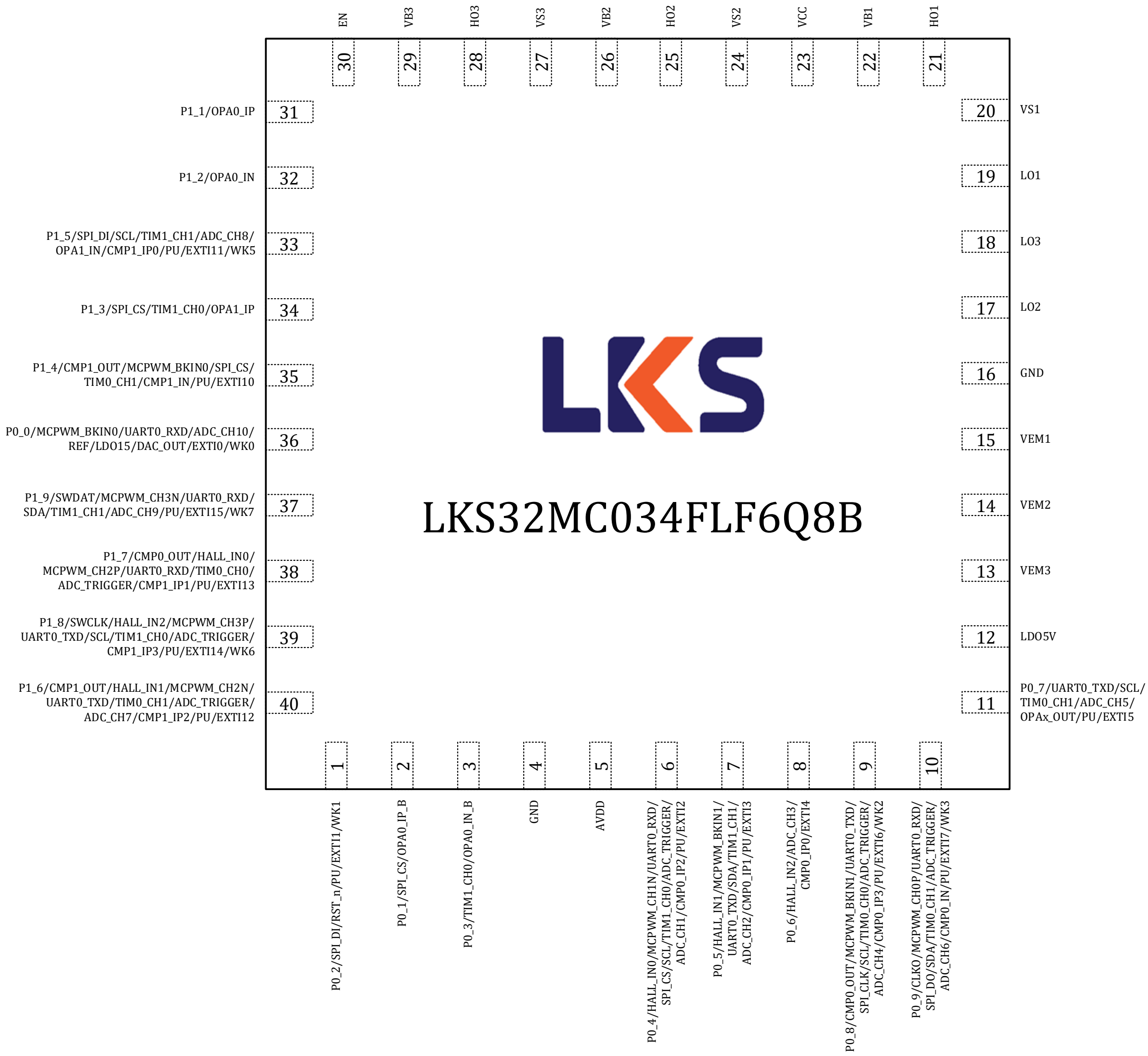

Figure 3-7 LKS32MC034FLF6Q8B(C) Pin Assignment Diagram

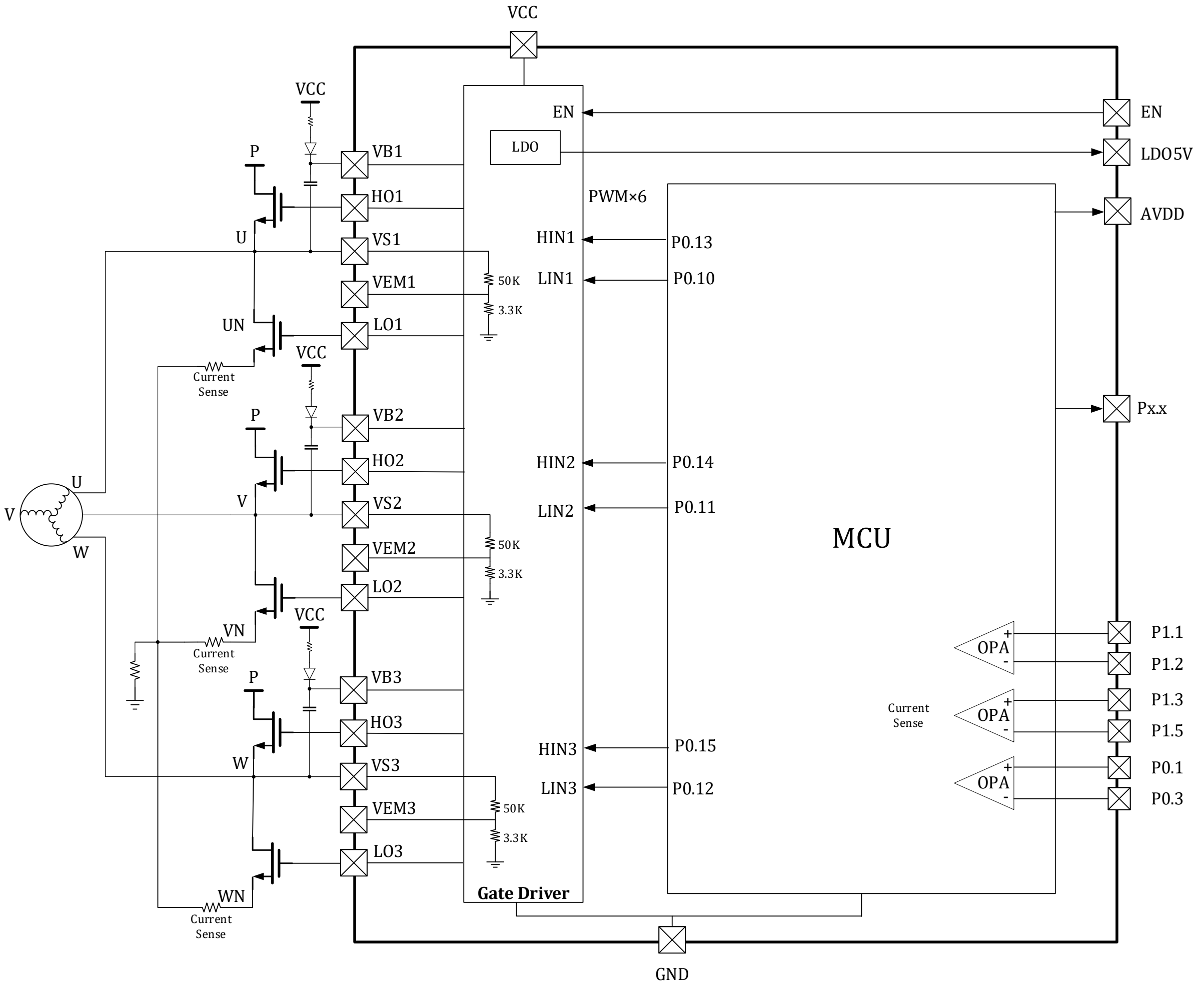

Figure 3-2 Schematic diagram of the LKS32MC034FLF6Q8B(C) gate driver connection

Table 3-8 LKS32MC034FLF6Q8B(C) Pin Description

0	GND	Chip ground, located on the belly of the chip
1	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
2	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
3	P0_3	P0.3
	TIM1_CH0	Timer1 channel0

	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
4	GND	Ground
5	AVDD	Power supply, 2.2~5.5V
6	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
7	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
8	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
9	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2

10	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
11	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
12	LDO5V	5V LDO output
13	VEM3	C phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
14	VEM2	B phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
15	VEM1	A phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
16	GND	Ground
17	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
20	VS1	High-side floating bias voltage 1.
21	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
22	VB1	High-side floating supply voltage 1.
23	VCC	Gate driver power supply

24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VS3	High-side floating bias voltage 3.
28	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
29	VB3	High-side floating supply voltage 3.
30	EN	Grid drive enabled， high level enables the predrive output，Low level turns off output，Built-in pull-up resistor, pull-up to 5V.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output

	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
37	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
38	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2

	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.10 LKS32MC034FLK6Q8C

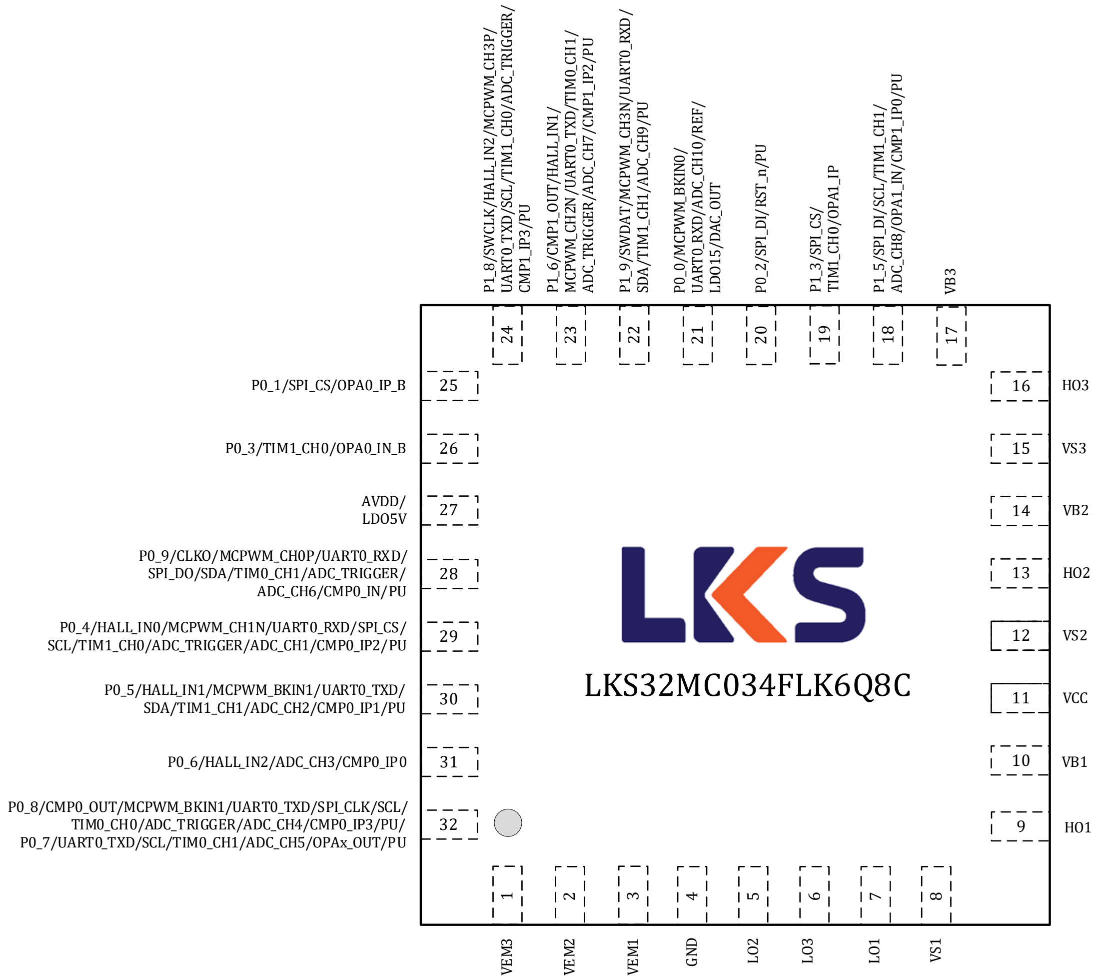

Figure 3-9 LKS32MC034FLK6Q8C Pin Assignment Diagram

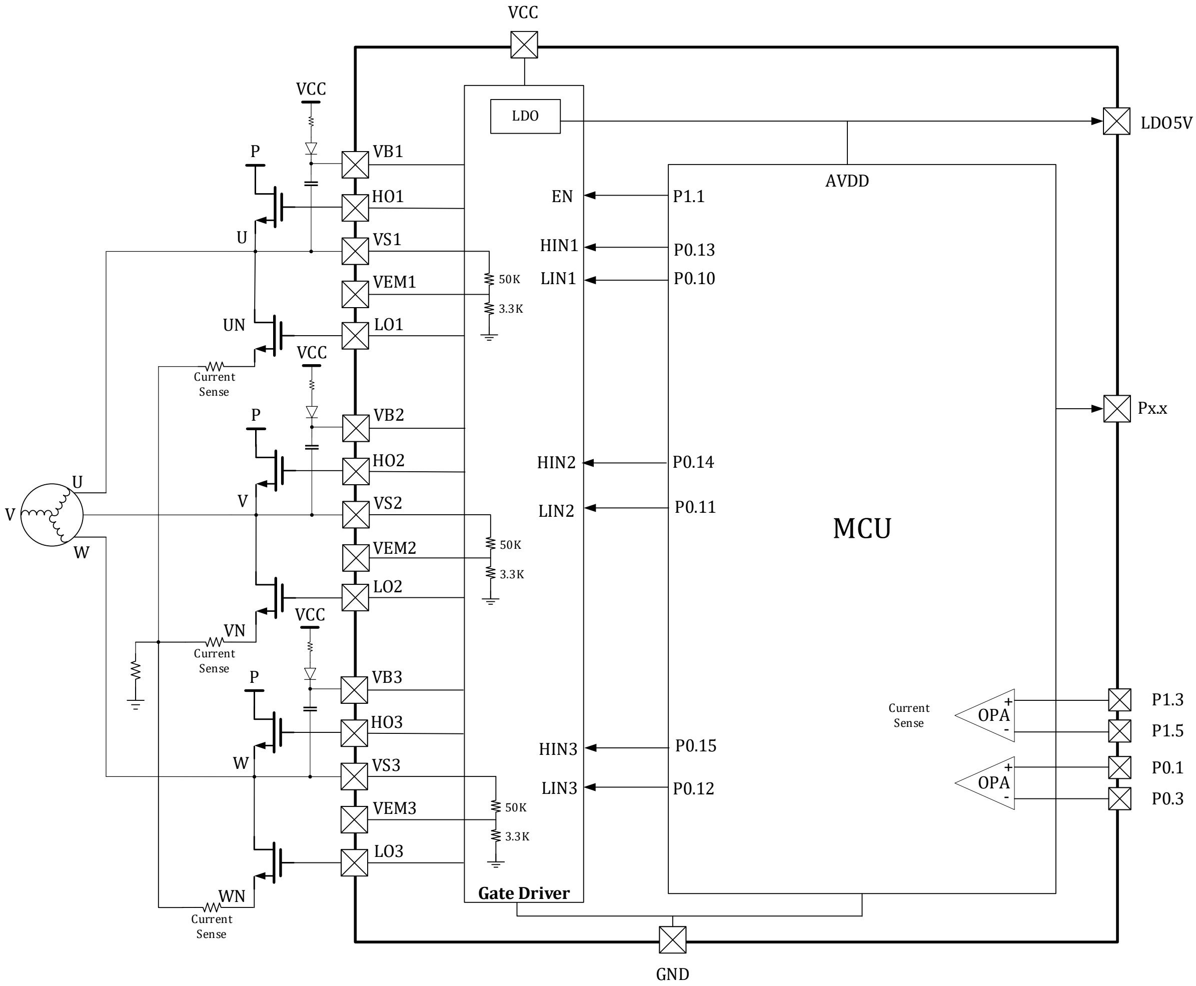

Figure 3-2 Schematic diagram of the LKS32MC034FLK6Q8C gate driver connection

Table 3-10 LKS32MC034FLK6Q8C Pin Description

0	GND	Chip ground, located on the belly of the chip
1	VEM3	C phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
2	VEM2	B phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
3	VEM1	A phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
4	GND	Ground
5	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
6	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO1 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.

7	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO3 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
8	VS1	High-side floating bias voltage 1.
9	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO3 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
10	VB1	High-side floating supply voltage 1.
11	VCC	Gate driver power supply
12	VS2	High-side floating bias voltage 2.
13	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
14	VB2	High-side floating supply voltage 2.
15	VS3	High-side floating bias voltage 3.
16	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
17	VB3	High-side floating supply voltage 3.
18	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal11
	WK5	External wake-up signal5
19	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
20	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal1
	WK1	External wake-up signal1
21	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug

	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal0
	WK0	External wake-up signal0
22	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal15
	WK7	External wake-up signal7
23	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal12
24	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal14
	WK6	External wake-up signal6
25	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
26	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1

27	AVDD	MCU power supply
	LDO5V	5V LDO output
28	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal7
	WK3	External wake-up signal3
29	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal2
30	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal3
31	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal4
32	P0_8	P0.8

	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal6
	WK2	External wake-up signal2
	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal5

3.1.11 LKS32MC034F2LF6Q8C

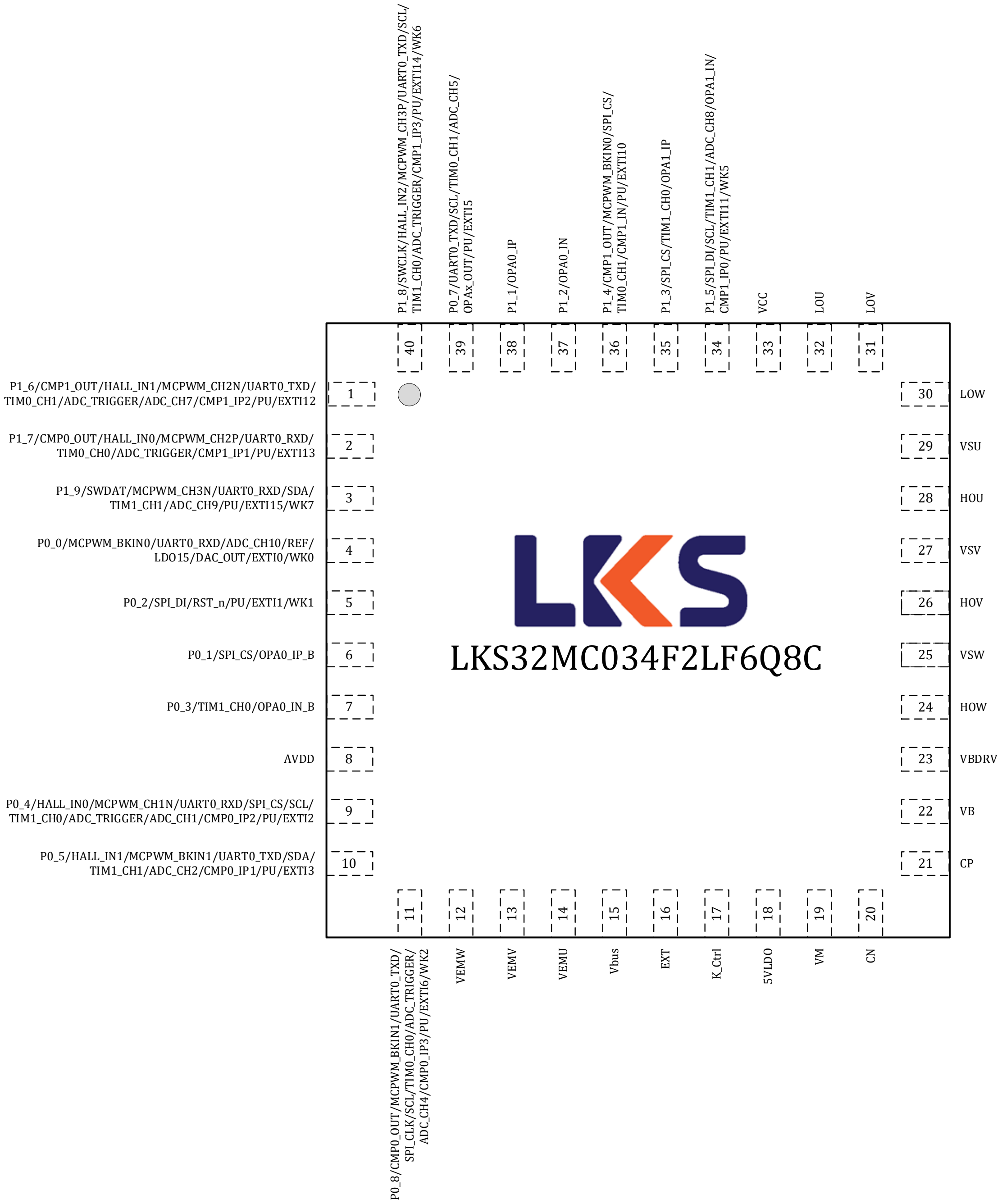

图 3-17 LKS32MC034F2LF6Q8C 管脚分布图

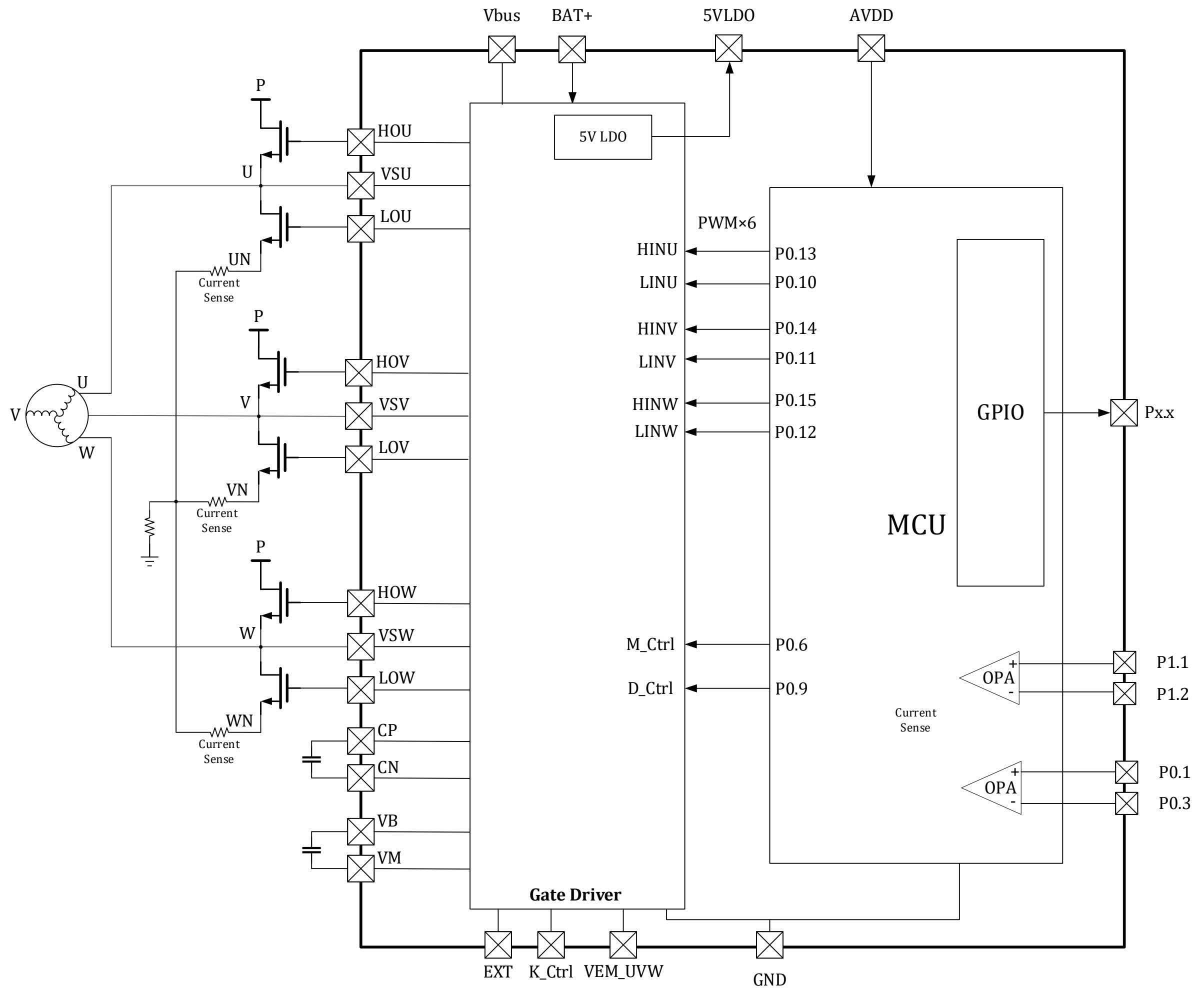

图 3-18 LKS32MC034F2LF6Q8C 预驱连接示意图

表 3-10 LKS32MC034F2LF6Q8C 管脚说明

	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
1	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal12
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
2	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)

	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal13
3	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal15
	WK7	External wake-up signal7
4	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal0
	WK0	External wake-up signal0
5	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal1
	WK1	External wake-up signal1
6	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
8	AVDD	MCU power supply

9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal3
11	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal6
	WK2	External wake-up signal2
12	VEMW	W-phase VS divider resistor output pin
13	VEMV	V-phase VS divider resistor output pin
14	VEMU	U-phase VS divider resistor output pin
15	Vbus	Bus voltage sampling signal
16	EXT	External double-plug switch interface (EXT pad is left in the air when this function is not required)
17	K_Ctrl	Power-down hold circuit, power-on control interface, external electronic key control
18	5VLDO	5VLDO

19	VM	Charge Pump Input
20	CN	Negative plate of charge pump flying-power supply
21	CP	Positive plate of charge pump flying-power supply
22	VB	Charge Pump Output
23	VBDRV	HS pull-up power supply
24	HOW	W-phase high side output
25	VSW	W-channel high-side floating ground
26	HOV	V-phase high side output
27	VSV	V-channel high-side floating ground
28	HOU	U-phase high side output
29	VSU	U-channel high-side floating ground
30	LOW	W-phase low-side output
31	LOV	V-phase low-side output
32	LOU	U-phase low-side output
33	VCC+	Working power input
34	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal11
	WK5	External wake-up signal5
35	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
36	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal10
37	P1_2	P1.2
	OPA0_IN	OPA0 negative input
38	P1_1	P1.1
	OPA0_IP	OPA0 positive input
39	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)

	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal5
40	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal14
	WK6	External wake-up signal6

3.1.12 LKS32MC0342FLK6Q8C

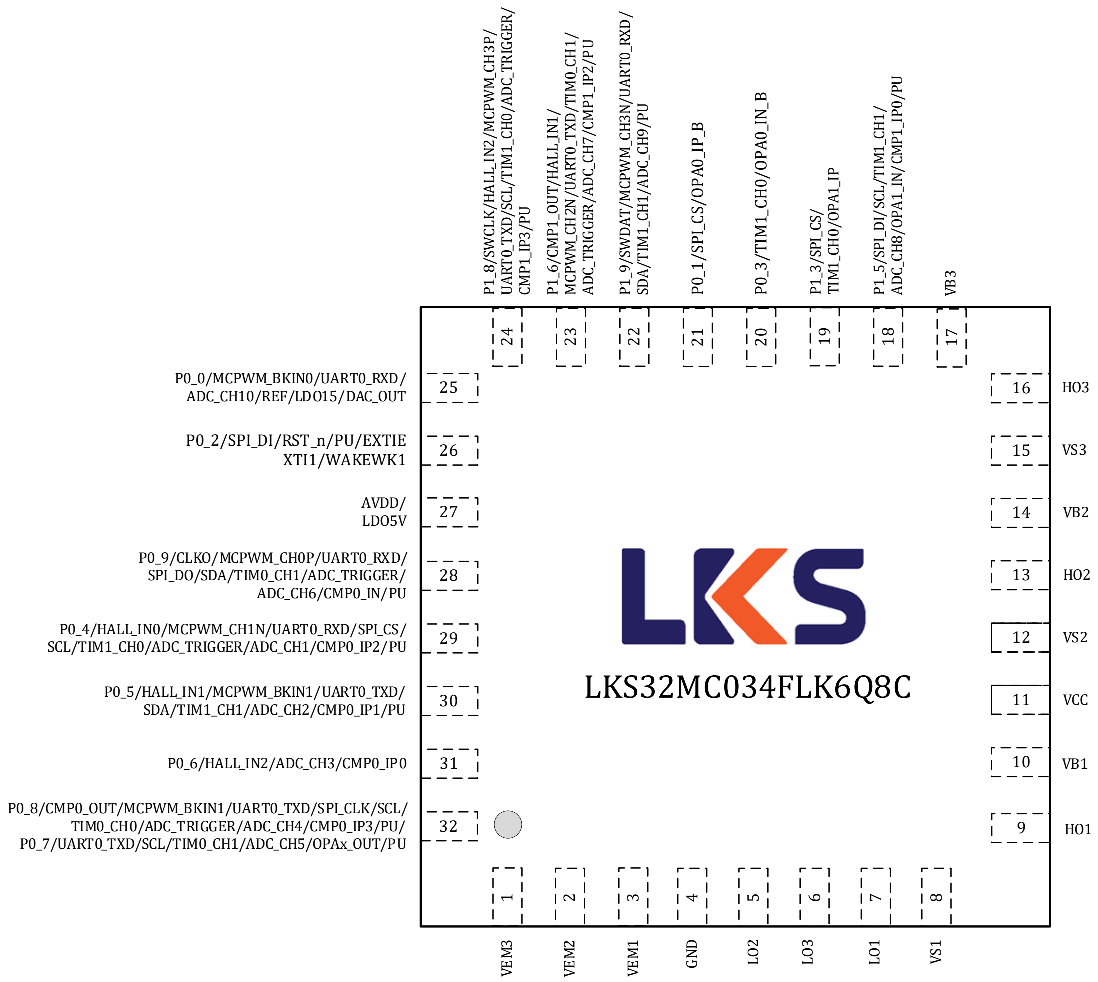

Figure 3-9 LKS32MC034FLK6Q8C Pin Assignment Diagram

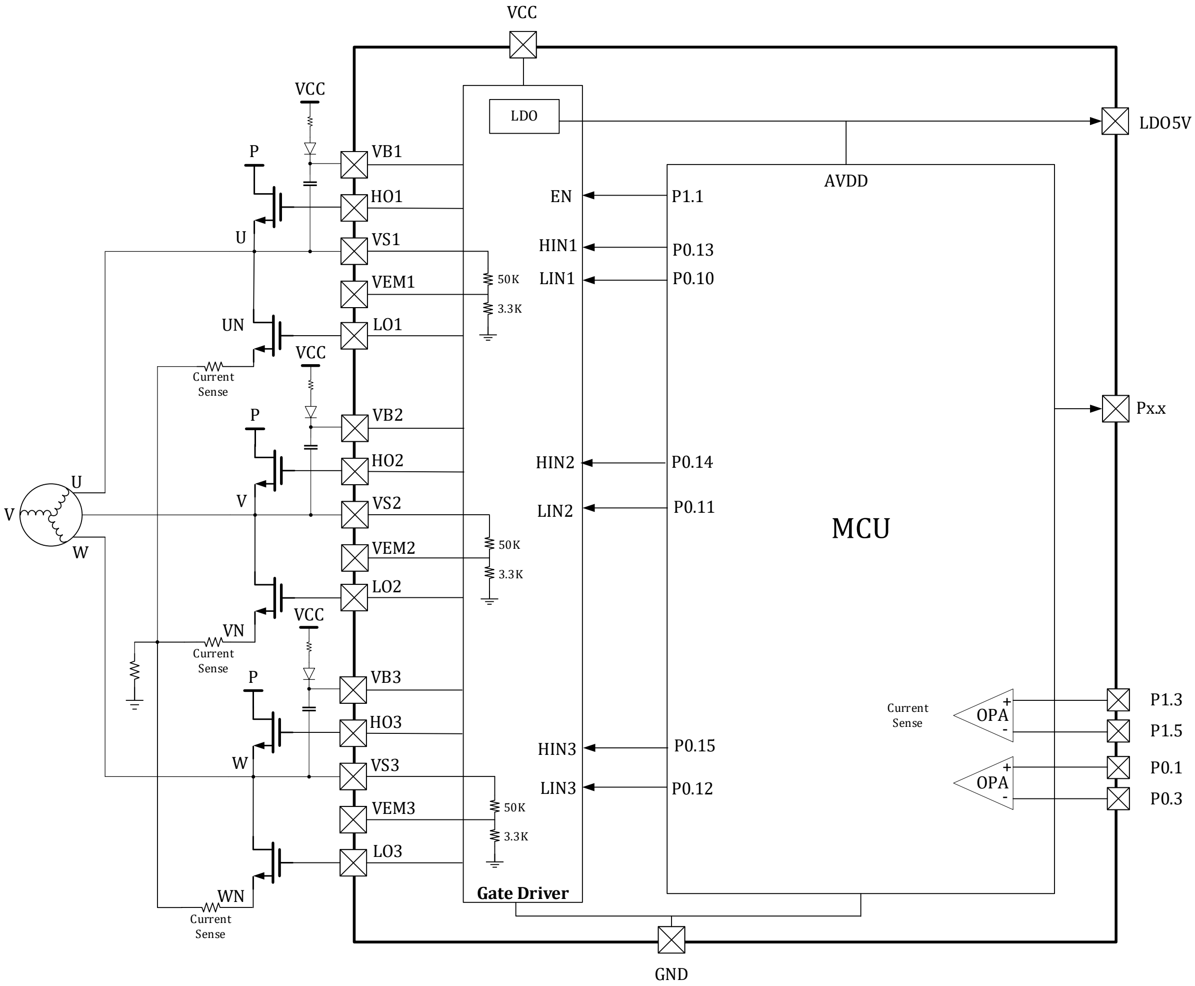

Figure 3-2 Schematic diagram of the LKS32MC034FLK6Q8C gate driver connection

Table 3-10 LKS32MC034FLK6Q8C Pin Description

0	GND	Chip ground, located on the belly of the chip
1	VEM3	C phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
2	VEM2	B phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
3	VEM1	A phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
4	GND	Ground
5	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
6	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO1 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
7	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO3 is the same as that

		of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
8	VS1	High-side floating bias voltage 1.
9	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO3 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
10	VB1	High-side floating supply voltage 1.
11	VCC	Gate driver power supply
12	VS2	High-side floating bias voltage 2.
13	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
14	VB2	High-side floating supply voltage 2.
15	VS3	High-side floating bias voltage 3.
16	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
17	VB3	High-side floating supply voltage 3.
18	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal11
	WK5	External wake-up signal5
19	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
20	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
21	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
22	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal15

	WK7	External wake-up signal7
23	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal12
24	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal14
	WK6	External wake-up signal6
25	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal0
	WK0	External wake-up signal0
26	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal1
	WK1	External wake-up signal1
27	AVDD	MCU power supply

	LDO5V	5V LDO output
28	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal7
	WK3	External wake-up signal3
29	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal2
30	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal3
31	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal4
32	P0_8	P0.8
	CMP0_OUT	Comparator 0 output

	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal6
	WK2	External wake-up signal2
	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal5

3.1.13 LKS32MC034F2LM6Q8C

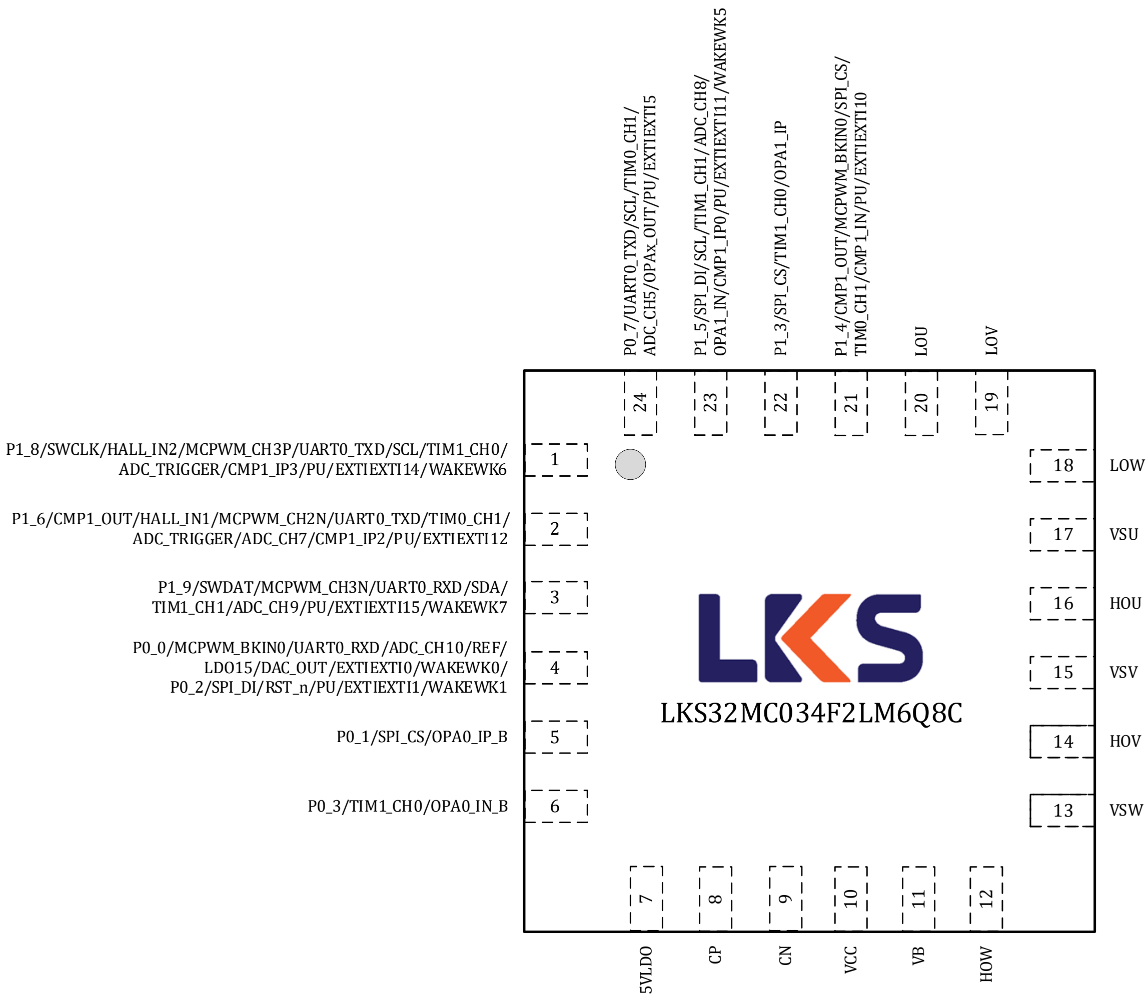

图 3-21 LKS32MC034F2LM6Q8C 管脚分布图

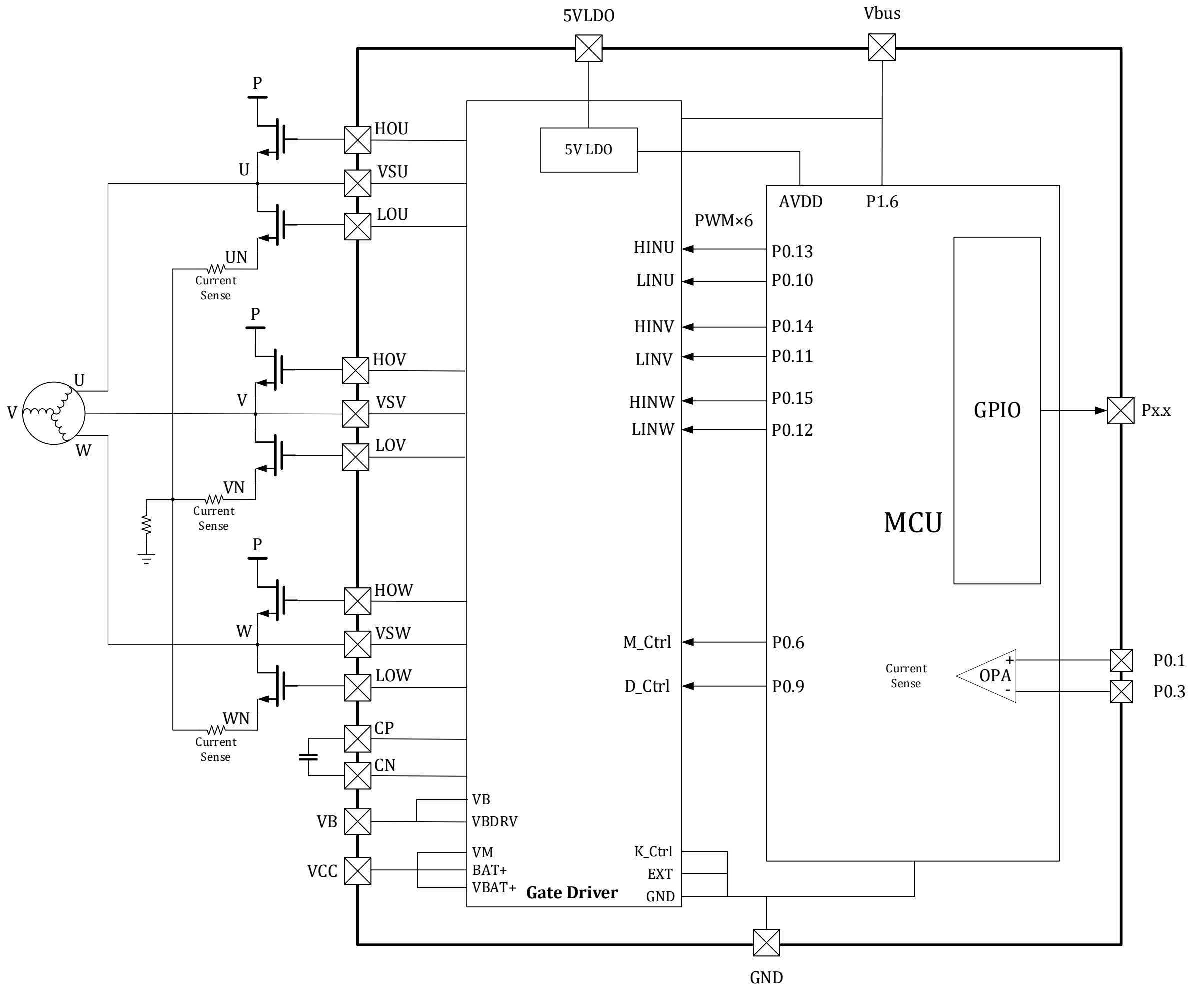

图 3-22 LKS32MC034F2LM6Q8C 预驱连接示意图

表 3-12 LKS32MC034F2LM6Q8C 管脚说明

1	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal14
	WK6	External wake-up signal6
2	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side

	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal12
3	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal15
	WK7	External wake-up signal7
4	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal0
	WK0	External wake-up signal0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal1
	WK1	External wake-up signal1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	5VLDO	5VLDO
8	CP	Positive plate of charge pump flying-power supply

9	CN	Negative plate of charge pump flying-power supply
10	VCC	Working power input
11	VB	Charge Pump Output
12	HOW	W-phase high side output
13	VSW	W-channel high-side floating ground
14	HOV	V-phase high side output
15	VSV	V-channel high-side floating ground
16	HOU	U-phase high side output
17	VSU	U-channel high-side floating ground
18	LOW	W-phase low-side output
19	LOV	V-phase low-side output
20	LOU	U-phase low-side output
21	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal10
22	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
23	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal11
	WK5	External wake-up signal5
24	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal5

3.1.14 LKS32MC034FLNK6Q8C

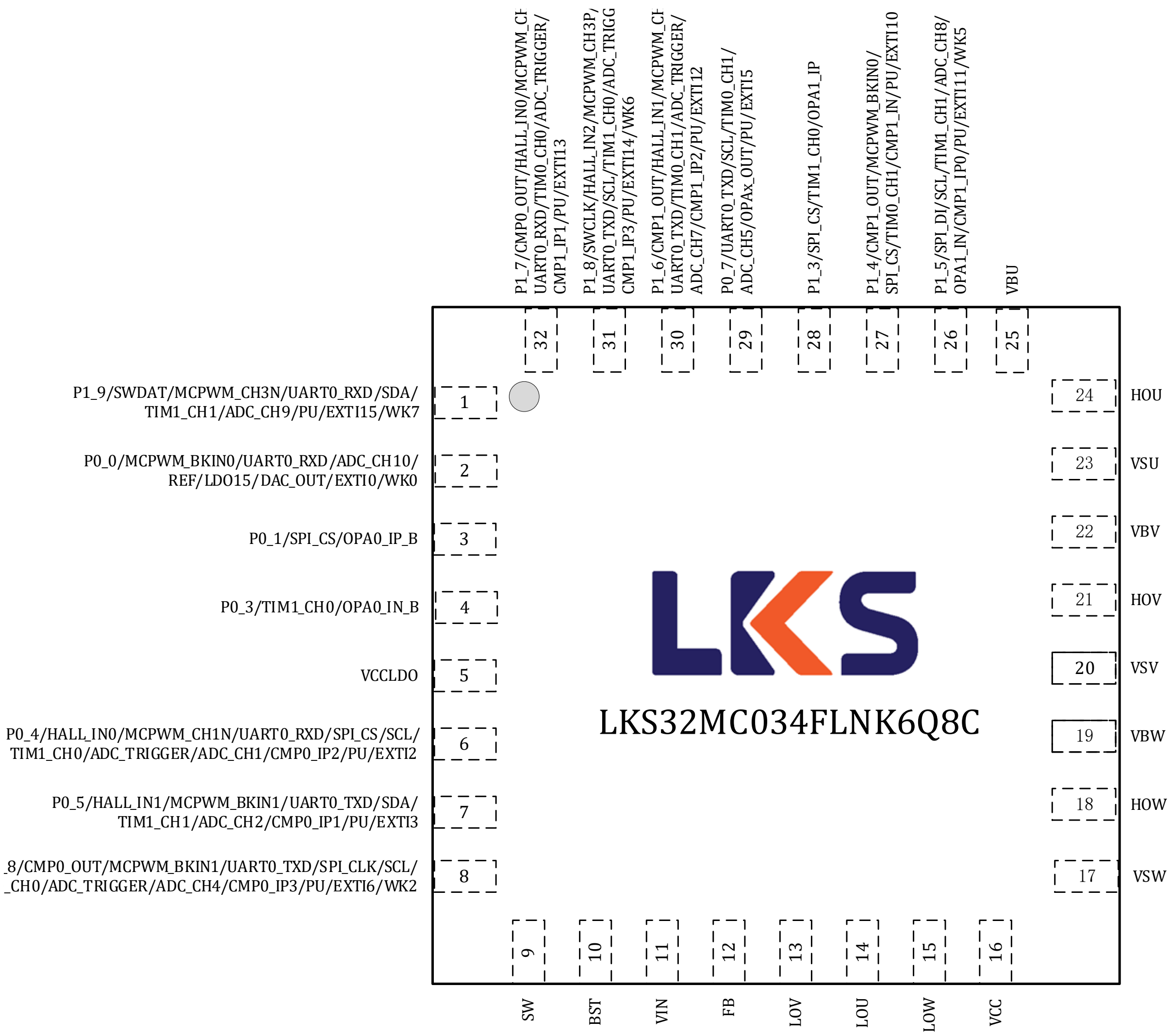

图 3-23 LKS32MC034FLNK6Q8C 管脚分布图

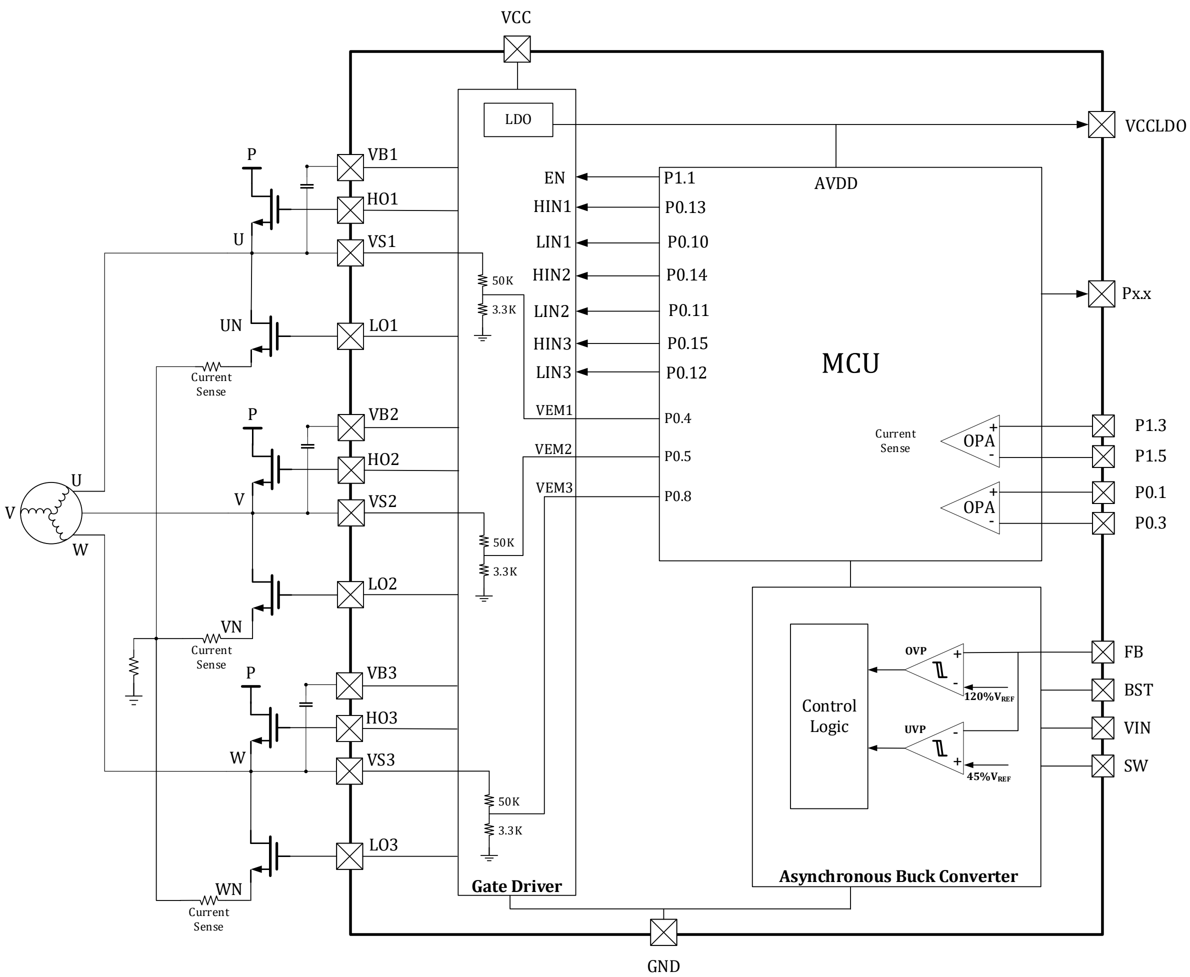

图 3-24 LKS32MC034FLNK6Q8C 预驱连接示意图

表 3-13 LKS32MC034FLNK6Q8C 管脚说明

1	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal15
	WK7	External wake-up signal7
2	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output

	EXTI0	External GPIO interrupt input signal0
	WK0	External wake-up signal0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal1
	WK1	External wake-up signal1
3	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
4	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
5	VCCLDO	5V LDO power supply
6	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal2
	VEM1	A phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
7	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal3

	VEM2	B phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
8	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal6
	WK2	External wake-up signal2
	VEM3	C phase VS 50k/3.3k cascaded resistor voltage devided output, built-in voltage 5V 30pF capacitor. The voltage ratio can be adjusted by adding external shunt resistor. If the voltage exceeds 5V, the sampled signal will be clamped by diode
9	SW	Regulator Switch Output.Connect SW to the external power inductor.
10	BST	Supply bias for the high-side power MOSFET gate driver.
11	VIN	Power supply input
12	FB	Inverting Input of the Comparator
13	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
14	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
15	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
16	VCC	Gate driver power supply
17	VS3	High-side floating bias voltage 3.
18	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
19	VB3	High-side floating supply voltage 3.
20	VS2	High-side floating bias voltage 2.
21	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
22	VB2	High-side floating supply voltage 2.
23	VS1	High-side floating bias voltage 1.
24	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
25	VB1	High-side floating supply voltage 1.
26	P1_5	P1.5

	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal11
	WK5	External wake-up signal5
27	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal10
28	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
29	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal5
30	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal12
31	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2

	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal14
	WK6	External wake-up signal6
32	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal13

3.1.15 LKS32MC034F2LNK6Q8C

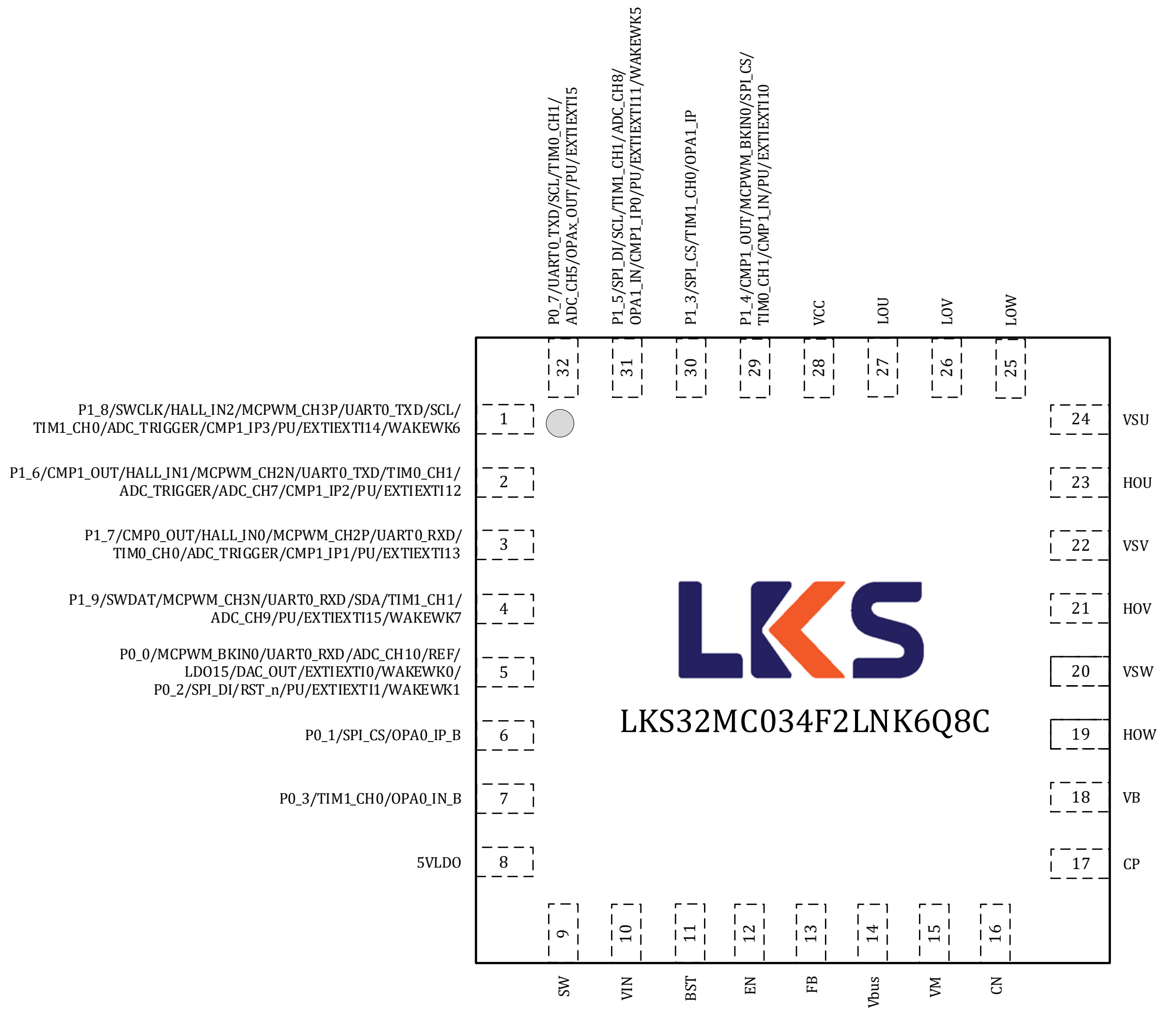

图 3-25 LKS32MC034F2LNK6Q8C 管脚分布图

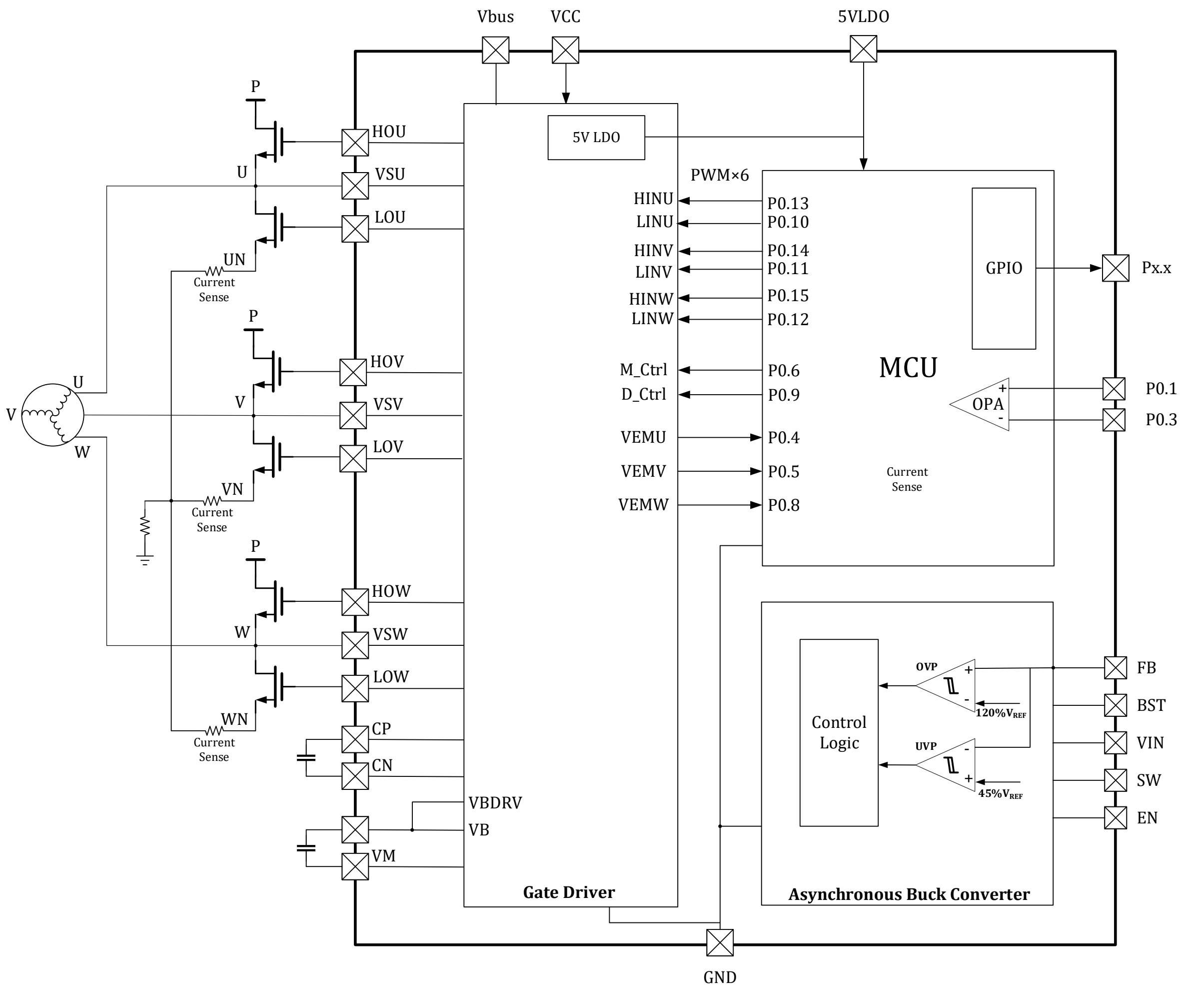

图 3-26 LKS32MC034F2LNK6Q8C 预驱连接示意图

表 3-14 LKS32MC034F2LNK6Q8C 管脚说明

1	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal14
	WK6	External wake-up signal6
2	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)

	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal12
3	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal13
4	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal15
	WK7	External wake-up signal7
5	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal0
	WK0	External wake-up signal0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal1

	WK1	External wake-up signal1
6	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
8	5VLDO	MCU power supply
9	SW	Regulator Switch Output.Connect SW to the external power inductor.
10	VIN	Power supply input
11	BST	Supply bias for the high-side power MOSFET gate driver.
12	EN	Inverting Input of the Comparator
13	FB	Bus voltage sampling signal
14	Vbus	Bus voltage sampling signal
15	VM	Charge Pump Input
16	CN	Negative plate of charge pump flying-power supply
17	CP	Positive plate of charge pump flying-power supply
18	VB	HS pull-up power supply
19	HOW	W-phase high side output
20	VSW	W-channel high-side floating ground
21	HOV	V-phase high side output
22	VSV	V-channel high-side floating ground
23	HOU	U-phase high side output
24	VSU	U-channel high-side floating ground
25	LOW	W-phase low-side output
26	LOV	V-phase low-side output
27	LOU	U-phase low-side output
28	VCC	Working power input
29	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal10
30	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
31	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock

	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal11
	WK5	External wake-up signal5
32	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal15

3.1.16 LKS32MC038KU6Q8B/ LKS32MC038KU6Q8C

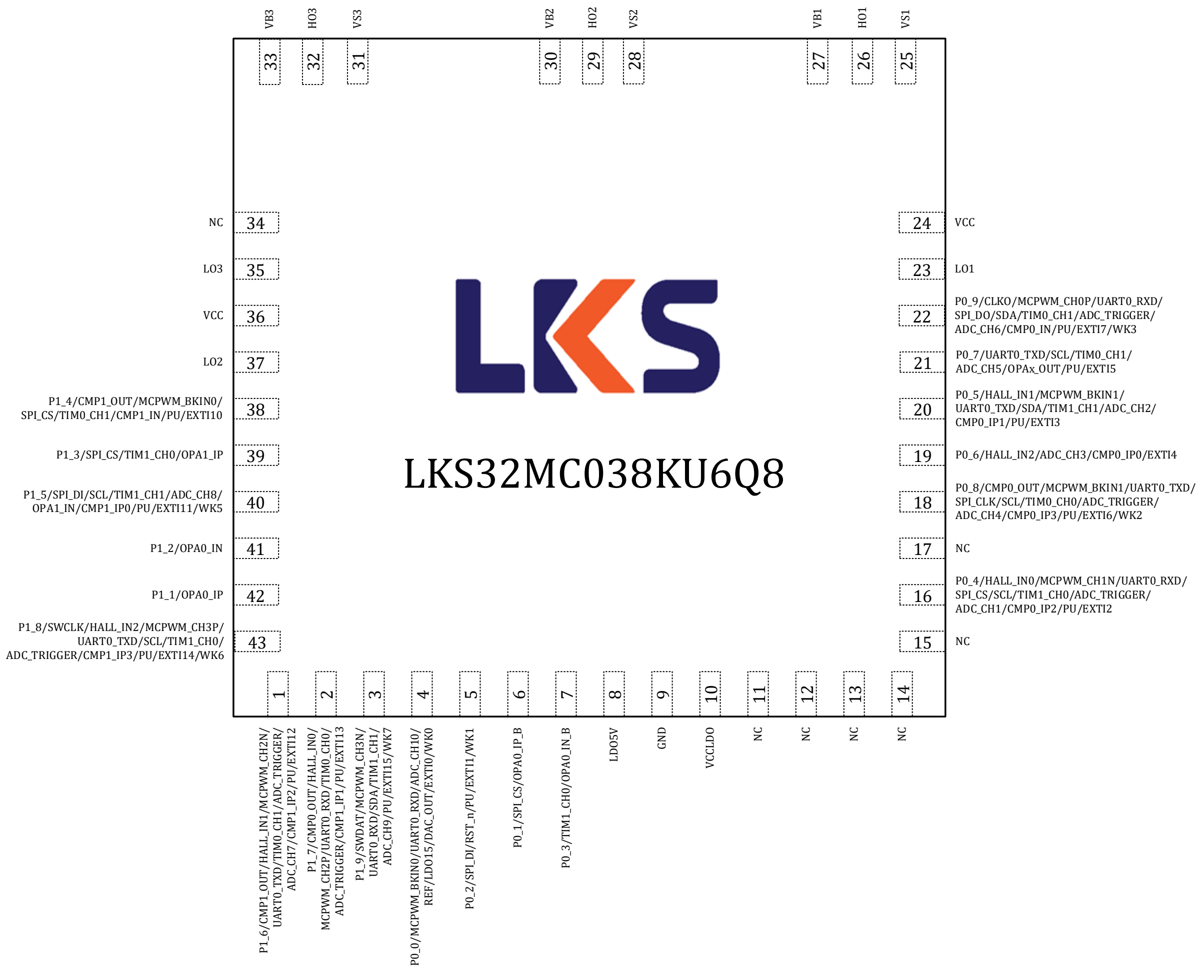

Figure 3-8 LKS32MC038KU6Q8B(C) Pin Assignment Diagram

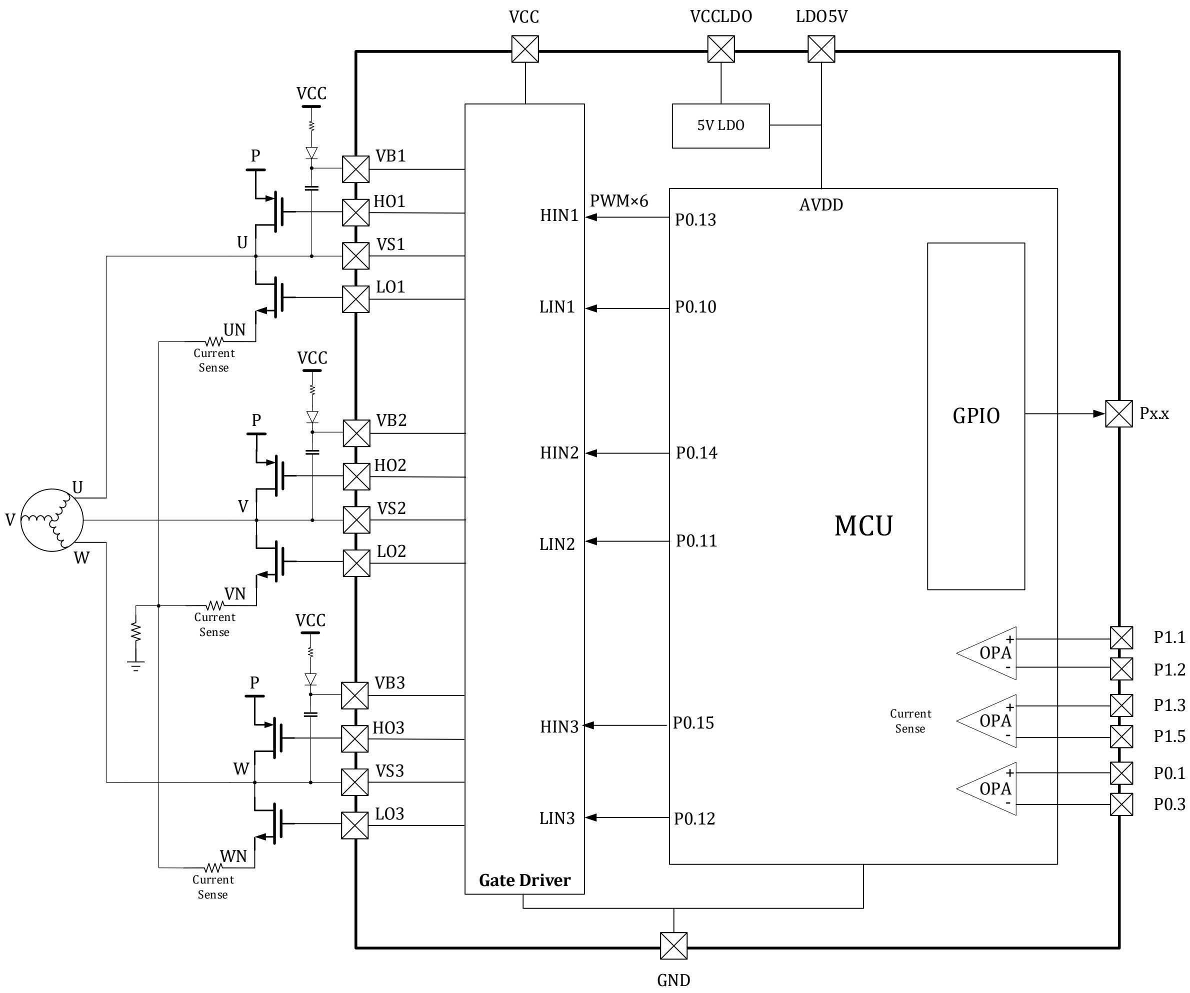

Figure 3-2 Schematic diagram of the LKS32MC038KU6Q8B(C) gate driver connection

Table 3-9 LKS32MC038KU6Q8B(C) Pin Description

0	GND	Chip ground, located on the belly of the chip
1	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
2	P1_7	P1.7
	CMP0_OUT	Comparator 0 output

	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
3	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
4	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
5	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
6	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
8	AVDD	5V LDO voltage output

9	GND	Ground
10	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
17	NC	Not connected
18	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
19	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
20	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)

	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
21	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
22	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
23	LO1	Phase A low-side output, worked by MCU P0.11; the polarity of LO1 is the same as that of P0.11, i.e. when P0.11 = 1, LO1 = 1. You need to set MCPWM_SWAP = 0.
24	VCC	Gate driver power supply
25	VS1	High-side floating bias voltage 1.
26	HO1	Phase A high-side output, worked by MCU P0.10; the polarity of HO1 is the same as that of P0.10, i.e. when P0.10 = 1, HO1 = 1. You need to set MCPWM_SWAP = 0.
27	VB1	High-side floating supply voltage 1.
28	VS2	High-side floating bias voltage 2.
29	HO2	Phase B high-side output, worked by MCU P0.12; the polarity of HO2 is the same as that of P0.12, i.e. when P0.12 = 1, HO2 = 1. You need to set MCPWM_SWAP = 0.
30	VB2	High-side floating supply voltage 2.
31	VS3	High-side floating bias voltage 3.
32	HO3	Phase C high-side output, worked by MCU P0.14; the polarity of HO3 is the same as that of P0.14, i.e. when P0.14 = 1, HO3 = 1. You need to set MCPWM_SWAP = 0.
33	VB3	High-side floating supply voltage 3.
34	NC	Not connected

35	LO3	Phase C low-side output, worked by MCU P0.15; the polarity of LO3 is the same as that of P0.15, i.e. when P0.15 = 1, LO3 = 1. You need to set MCPWM_SWAP = 0.
36	VCC	Gate driver power supply
37	LO2	Phase B low-side output, worked by MCU P0.13; the polarity of LO2 is the same as that of P0.13, i.e. when P0.13 = 1, LO2 = 1. You need to set MCPWM_SWAP = 0.
38	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
39	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
40	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
41	P1_2	P1.2
	OPA0_IN	OPA0 negative input
42	P1_1	P1.1
	OPA0_IP	OPA0 positive input
43	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6

3.2 Pin Multiplexing

The table below shows the pin function reuse for version C.Please refer to 3.1.2 for the function difference of A/B version.

Table 3-3 LKS32MC03x Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					SPI_CS					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								TIM1_CH0		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD		SDA		TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	ADC_CH6/CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		ADC_CH8/OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	ADC_CH7/CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			TIM0_CH0		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

Table 3-3 LKS32MC03xB Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					SPI_CS					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								TIM1_CH0		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD				TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	ADC_CH6/CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		ADC_CH8/OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	ADC_CH7/CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			TIM0_CH0		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

4 Package Dimensions

4.1 LKS32MC031KLC6T8B/ LKS32MC031KLC6T8C

LQFP48L 0707 Profile Quad Flat Package:

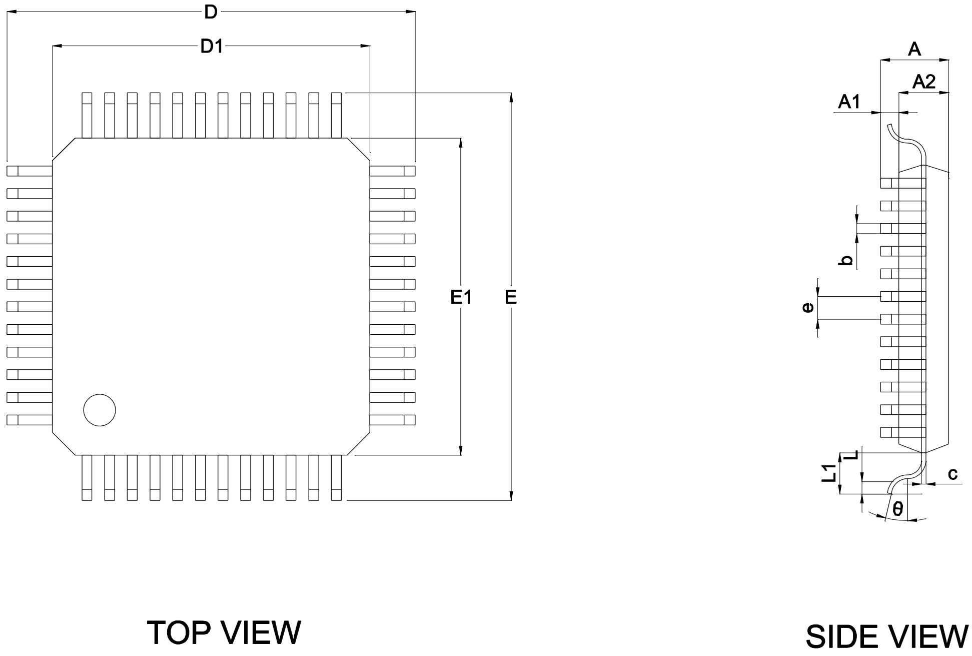

Figure 4-1 LKS32MC031KLC6T8B(C) Packaging

Table 4-1 LKS32MC031KLC6T8B(C) Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.19	0.22	0.27
c	0.13	-	0.17
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	-	1.00	-

4.2 LKS32MC034D(O)F6Q8(B/C)/LKS32MC034SF6Q8(B/C)/ LKS32MC034FLF6Q8B(C) /LKS32MC034F2LF6Q8C /LKS32MC034S2F6Q8B(C)

QFN5*5 40L-0.75 Profile Quad Flat Package:

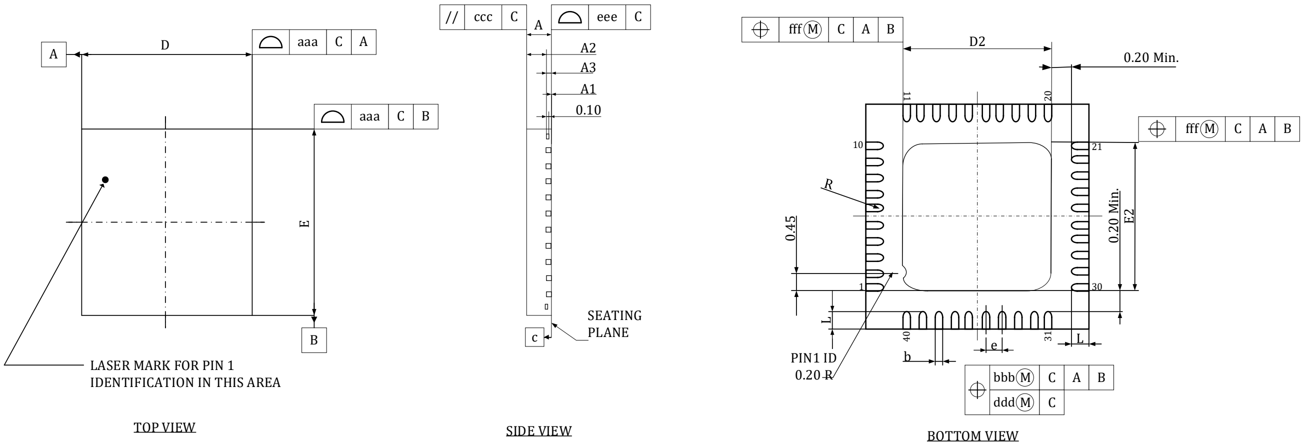

Figure 4-2 LKS32MC034D(O)F6Q8(B/C)/LKS32MC034SF6Q8(B/C)/LKS32MC034FLF6Q8B(C) /LKS32MC034F2LF6Q8C /LKS32MC034S2F6Q8B(C) Packaging

Table 4-2 LKS32MC034D(O)F6Q8(B/C)/LKS32MC034SF6Q8(B/C)/LKS32MC034FLF6Q8B(C) /LKS32MC034F2LF6Q8C /LKS32MC034S2F6Q8B(C) Package Dimensions

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.95	0.028	0.030	0.037
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	0.50	0.55	0.75	0.020	0.022	0.030
A3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	3.20	3.70	3.80	0.126	0.146	0.150
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.20	3.70	3.80	0.126	0.146	0.150
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.4 bsc			0.016 bsc		
R	0.075	-	-	0.003	-	-
TOLERANCE OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

4.3 LKS32MC038KU6Q8B/ LKS32MC038KU6Q8C

QFN43L Profile Quad Flat Package:

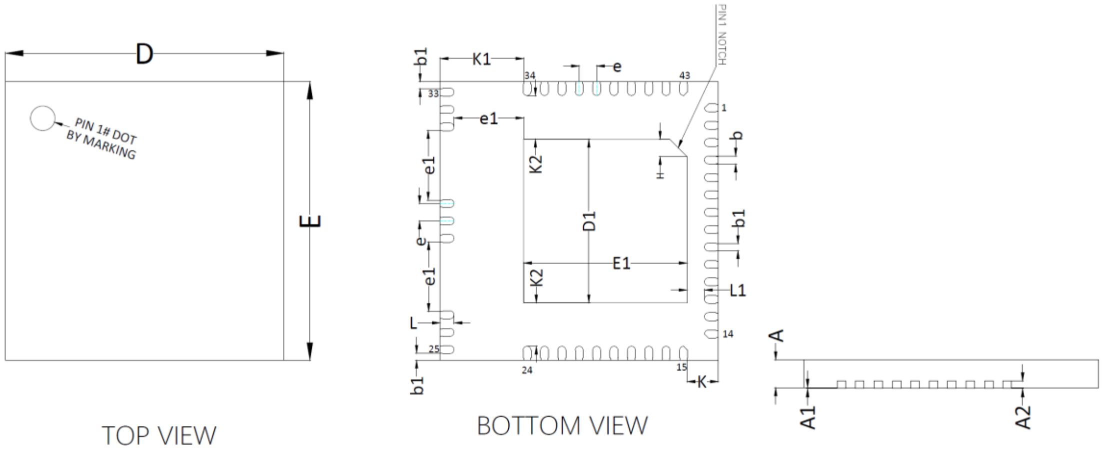

Figure 4-3 LKS32MC038KU6Q8B(C) Packaging

Table 4-3 LKS32MC038KU6Q8B(C) Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2	0.203REF		
b	0.18	0.23	0.28
b1	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	0.50BSC		
e1	2.00BSC		
D1	4.60	4.70	4.80
E1	4.60	4.70	4.80
L	0.30	0.40	0.50
L1	0.45	0.50	0.55
K	0.90BSC		
K1	2.40BSC		
K2	1.25BSC		
H	0.50BSC		

4.4 LKS32MC034FLK6Q8C/LKS32MC0342FLK6Q8C/LKS32MC034FLNK6Q8C/LKS32MC034F2LNK6Q8C

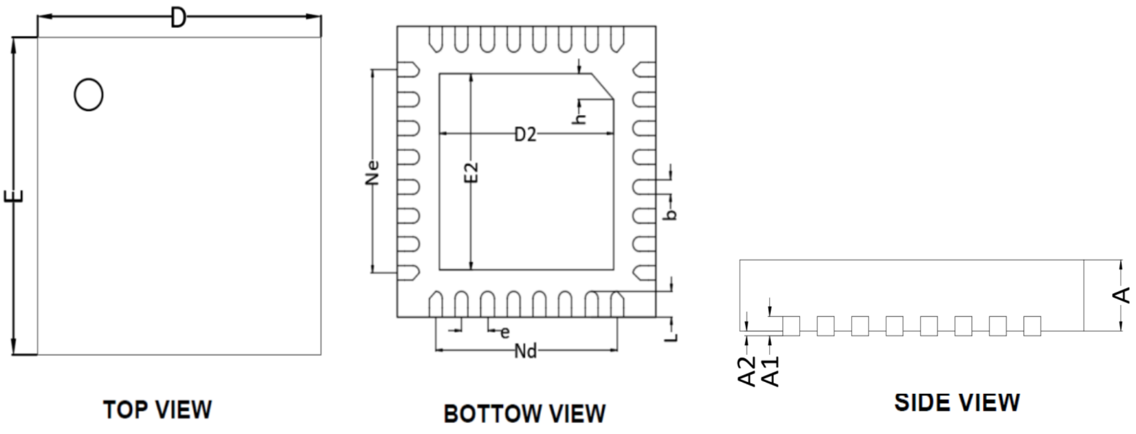

Figure 4-4

LKS32MC034FLK6Q8C/LKS32MC0342FLK6Q8C/LKS32MC034FLNK6Q8C/LKS32MC034F2LNK6Q8C

Packaging

Table 4-4

LKS32MC034FLK6Q8C/LKS32MC0342FLK6Q8C/LKS32MC034FLNK6Q8C/LKS32MC034F2LNK6Q8C

Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.203 REF		
A2	0.00	0.02	0.05
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.40 BSC		
Ne	2.80 BSC		
Nd	2.80 BSC		
L	0.30	0.35	0.40
B	0.15	0.20	0.25
h	0.30	0.35	0.40

4.5 LKS32MC034F2LM6Q8C

QFN4*4 24L-0.75。

Profile Quad Flat Package:

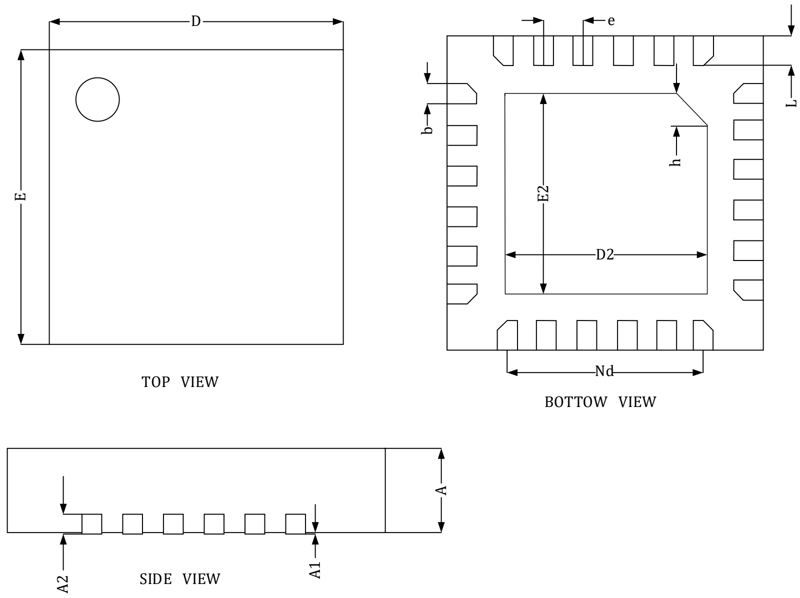

Figure 4-5 LKS32MC034F2LM6Q8C Packaging

Table 4-5 LKS32MC034F2LM6Q8C Package Dimensions

SYMBOL	MLLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
Nd	2.50 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
b	0.20	0.25	0.30
h	0.30	0.35	0.40

5 Electrical Characteristics

Table 5-1 LKS32MC03x 6N Electrical Limit Parameter

Parameter	Min.	Max.	Unit	Description
MCU Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Supply Voltage (VCC1/VCC2/VCC)	-0.3	+48.0	V	LKS32MC034F2LM6Q8C LKS32MC034F2LNK6Q8C LKS32MC034F2LF6Q8C
	-0.3	+25.0	V	LKS32MC031KLC6T8(B/C) LKS32MC034DF6Q8(B/C) LKS32MC034DOF6Q8(B/C)
	-0.3	+22.0	V	LKS32MC034FLF6Q8B/C LKS32MC034FLK6Q8C LKS32MC034SF6Q8(B/C) LKS32MC034S2F6Q8(B/C) LKS32MC034FLNK6Q8C
LDO Supply Voltage (VCCLDO)	-0.3	+25.0	V	LDO Powered Pin
5V LDO Output Current		80	mA	LKS32MC031KLC6T8(B/C) LKS32MC034DOF6Q8(B/C) LKS32MC034SF6Q8(B/C)
		30	mA	LKS32MC034FLF6Q8(B/C) LKS32MC034FLK6Q8C LKS32MC034SF6Q8(B/C) LKS32MC034S2F6Q8(B/C)
	50	200	mA	LKS32MC034F2LF6Q8C LKS32MC034F2LM6Q8C LKS32MC034FLNK6Q8C LKS32MC034F2LNK6Q8C
Operating temperature	-40	+105	˚C	
Storage temperature	-40	+150	˚C	
Junction temperature	-	125	°C	
Pin temperature	-	260	°C	Soldering for 10 sec

Table 5-2 LKS32MC03x 6N Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
MCU Supply Voltage (AVDD)	2.5	5	5.5	V	
Analog Operating Voltage ($AVDD_A$)	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Gate Driver Supply Voltage (VCC)	4.5		20	V	LKS32MC034FLF6Q8(B/C) LKS32MC034FLK6Q8C LKS32MC034SF6Q8(B/C)

					LKS32MC034S2F6Q8(B/C)
	7				LKS32MC034DF6Q8(B/C) LKS32MC034DOF6Q8(B/C)
	13				LKS32MC031KLC6T8(B/C)
	10				LKS32MC038KU6Q8(B/C)
	5		40	V	LKS32MC034F2LM6Q8C LKS32MC034F2LF6Q8C LKS32MC034F2LN2K6Q8C LKS32MC034F2LNK6Q8C
LDO Supply Voltage (VCCLDO)	7		20	V	LDO power supply

OPA could work under 2.5V, but the output range will be limited.

Table 5-3 LKS32MC03x 6N ESD parameters

Item	Chip model	Pin	Min.	Max.	Unit
ESD test (HBM)	LKS32MC031KLC6T8(B/C)	MCU	-6000	6000	V
		PWR	-4000	4000	V
		Gate driver	-2000	2000	V
	LKS32MC034DF6Q8(B/C)	MCU	-6000	6000	V
		Gate driver	-2000	2000	V
	LKS32MC034DOF6Q8(B/C)	MCU	-6000	6000	V
		PWR	-4000	4000	V
		Gate driver	-2000	2000	V
	LKS32MC034SF6Q8(B/C) LKS32MC034FLF6Q8(B/C) LKS32MC034FLK6Q8C LKS32MC0342FLK6Q8C LKS32MC034F2LF6Q8C LKS32MC034F2LM6Q8C	MCU	-6000	6000	V
		Gate driver	-2500	2500	V
	LKS32MC038KU6Q8(B/C)	MCU	-6000	6000	V
		Gate driver	-2000	2000	V
	LKS32MC034FLNK6Q8C LKS32MC034F2LNK6Q8C				

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC03x 6N Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

Table 5-5 LKS32MC03x 6N IO Limit Parameter

Parameter	Description	Minimum	Maximum	Unit
V_{IN}	Input voltage range for GPIO signals	-0.3	6.0	V
I_{INJ_PAD}	Maximum injection current for single GPIOs	-11.2	11.2	mA
I_{INJ_SUM}	Maximum injection current for all GPIOs	-50	50	mA

Table 5-6 LKS32MC03x 6N IO DC Parameter

Parameter	Description	AVDD	Conditions	Min.	Max.	Unit
V_{IH}	High input level of digital IO	5V	-	0.7*AVDD		V
		3.3V		2.0		
V_{IL}	Low input level of digital IO	5V	-		0.3*AVDD	V
		3.3V			0.8	
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD		V
		3.3V				
I_{IH}	Digital IO current consumption when input is high	5V	-		1	uA
		3.3V				
I_{IL}	Digital IO current consumption when input is low	5V	-	-1		uA
		3.3V				
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8		V
V_{OL}	Low output level of digital IO		Current = 11.2mA		0.5	V
R_{pup}	Pull-up resistor*			8	12	kΩ
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit			100	200	Ω
C_{IN}	Digital IO Input-capacitance	5V	-		10	pF
		3.3V				

* Only part of IOs have built-in pull-up resistors. Please refer to the pin description section for details

Table 5-7 LKS32MC03x 6N Current Consumption IDDQ

Clock	Operating mode	3.3V	5V	Unit
48MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules are active, IOs stay idle	8.570	8.650	mA
4MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules except PLL are active, IOs stay idle	3.012	3.165	mA
64kHz		2.445	2.618	mA
-	Deep Sleep Mode, PLL and BGP are turned off, only 64kHz LRC is running	27	30	uA

-	All analog modules	2.4	2.55	mA

Unless otherwise specified, the above tests are all measured at room temperature of 25°. Due to the deviation of the device model in the manufacturing process, the current consumption of different chips will have individual differences.

6 Analog Characteristics

The performance parameters of the MCU analog part are shown below.

Table 6-1 LKS32MC034DOF6Q8 Analog Characteristics

Parameter	Min.	Typ.	Max.	Unit	Description
ADC					
Supply voltage	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Output bitrate		1.2		MHz	$f_{adc}/20$
Differential input signal range	-2.352		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-3.528		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
Single-ended input signal range	-0.3		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-0.3		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
	-0.3		AVDD*0.9	V	REF2VDD=1, Gain=1; REF=AVDD
	-0.3		AVDD+0.3	V	REF2VDD=1, Gain=2/3 , REF=AVDD, limited by IO diode clamp
The differential signal is usually the signal output from the OPA inside the chip to the ADC; The single-ended signal is usually the sampled signal from the external input through IO. Whether using an internal/external reference, the signal amplitude should not exceed ±98% of the ADC signal range. In particular, when using an external reference, it is recommended that the sampled signal not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input resistance	500k			Ohm	
Input capacitance		10p		F	
Reference voltage (REF)					
Supply voltage	2.5	5	5.5	V	
Output deviation	-9		9	mV	
Power supply rejection ratio		70		dB	

Parameter	Min.	Typ.	Max.	Unit	Description
Temperature coefficient		20		ppm/°C	
Output voltage		2.4		V	
DAC					
Supply voltage	2.5	5	5.5	V	
Load resistance	50k			Ohm	
Load capacitance			50p	F	
Output voltage range	0.05		3.0	V	
Switching speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational amplifier (OPA)					
Supply voltage	3.1	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load resistance	20k			Ohm	
Load capacitance			5p	F	
Common-mode input range	0		AVDD	V	
Output signal range	0.1		AVDD-0.1	V	Minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification x OFFSET
Common Mode Voltage (Vcm)	1.65		2.15	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier

Parameter	Min.	Typ.	Max.	Unit	Description
					Differential and Single Operating Mode".
Common-mode rejection ratio (CMRR)		80		dB	
Power supply rejection ratio (PSRR)		80		dB	
Load current			500	uA	
Slew rate		5		V/us	
Phase margin		60		°	
Comparator (CMP)					
Supply voltage	2.5	5	5.5	V	
Input signal range	0		AVDD	V	
OFFSET		-12.92		mV	0 mV hysteresis, CMP output low-to-high inversion
		-12.12		mV	0 mV hysteresis, CMP output high-to-low inversion
		-11.63		mV	20 mV hysteresis, CMP output low-to-high inversion
		5.21		mV	20 mV hysteresis, CMP output high-to-low inversion
Transmission delay		0.15		uS	Default power consumption
		0.6		uS	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'
GPIO					
High Level Inversion Threshold	2.61		3.04	V	

LKS32MC031KLC6T8(B/C), LKS32MC034DOF6Q8 (B/C) internal integrated 5V LDO parameters are shown below.

Table 6-2 5V LDO Module Parameter

5V LDO					
Input power	7		20	V	
Output voltage	4.75	5	5.25	V	+/-5% accuracy
Dropout voltage		2		V	
Output current		80		mA	
Ripple rejection		80		dB	
Decoupling capacitor input		0.33		uF	It is added to the VCCLDO pin. Please refer to the pin description section for details
Decoupling capacitor output		1		uF	It is added to the AVDD pin. Please refer

					to the pin description section for details
Operating temperature range	-40		125	℃	

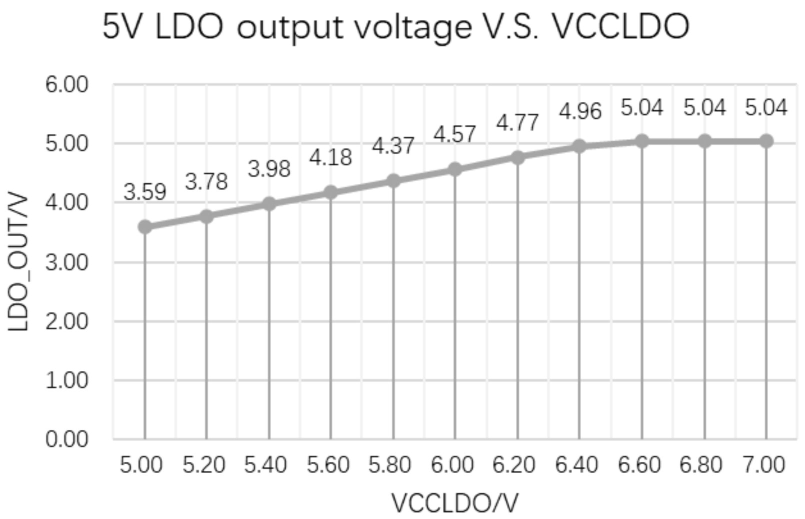

Figure 6-1 5V LDO Output Transfer Curve

LKS32MC034FLF6Q8(B/C),LKS32MC034FLK6Q8C,LKS32MC034SF6Q8(B/C), LKS32MC034S2F6Q8(B/C) internal integrated 5V LDO parameters refer to section 21.1.5.

Description of the analog register table:

The addresses 0x40000010-0x40000028 are the calibration registers for each module, which are provided with calibration values before being shipped from the factory. In general, you are not recommended to configure or change these values. To fine tune the analog parameters, you need to read the original calibration value.

The registers in the blank section must all be configured to 0 (reset to 0 when the chip is powered up). Other registers are configured as required by application scenarios.

7 Power Management System

The power management system consists of an LDO15 module and a power-on/power-off reset module (POR).The 5V LDO is integrated on select models.

7.1 AVDD

AVDD is a 5V LDO output for theLKS32MC031KLC6T8(B/C),LKS32MC034DOF6Q8(B/C), LKS32MC034SF6Q8(B/C), LKS32MC038KU6Q8(B/C),LKS32MC034FLK6Q8C chip. It is recommended that the off-chip decoupling capacitor be ≥ 1uF as close as possible to the AVDD pin.

For the LKS32MC034FLF6Q8(B/C) chip, LDO5V is the 5V LDO output, and AVDD is the chip power supply. If internal 5V LDO power supply is used, AVDD needs to be connected to LDO5V.

AVDD supplies power to the LDO15 module that powers all internal digital circuits and PLL modules.

LDO15 is automatically enabled after power-up and requires no software configuration, but the output voltage of LDO15 needs to be fine-tuned by software.

The output voltage of LDO15 can be adjusted by setting the register LDO15TRIM<2:0>. Please refer to the description of the analog register table for specific register values. LDO15 is calibrated before the chip is shipped from the factory, and generally, you do not need to configure these additional registers. To fine tune the output voltage of LDO, you need to read the original configuration value and fill in the configuration value corresponding to the fine-tuning amount.

The POR module monitors the voltage of LDO15 and provides a reset signal to the digital circuit when the LDO15 voltage falls below 1.1V (for example, at the beginning of power-up or during power-down), to avoid the abnormal operation of the digital circuit.

7.2 VCC

The on-chip driving module provides power supply.Refer to chapter 5 for voltage range.

7.3 VCCLDO

The VCCLDO pin in the LKS32MC031KLC6T8(B/C),LKS32MC034DOF6Q8(B/C), LKS32MC034SF6Q8(B/C), LKS32MC038KU6Q8(B/C) operates from 7-20V to power the on-chip 5V LDO module. If 5V AVDD is used for external power supply, the power supply current is limited to below 20mA.

External resistor selection for VCCLDO

Due to the nature of the linear power supply, heat generation on the LDO is noticeable when the input voltage is high (e.g.> = 15V) and the load current is large (e.g.> = 30mAV). It is likely that the chip will trigger thermal protection at an ambient temperature around 125 degrees or less.

The chip itself consumes less than 10mA at 5V. If the 5V LDO supplies more than 10mA to the periphery of the chip, a shunt resistor may be bridged across AVDD and VCCLDO.
The resistance value should be calculated according to the following formula:

R>=1.5*(VCCLDO-AVDD)/I

Where, I is the total power dissipated on the 5V supply, including the power dissipated by the MCU and that dissipated by the 5V peripheral devices such as HALL.

With an external shunt resistor bridged, a 5.6V regulator should be placed at the AVDD pin.

8 Timer System

The timer system consists of an internal 64kHz RC timer, an internal 4MHz RC timer, and a PLL circuit.

The 64k RC timer is used as an MCU slow timer, a filtration module or an MCU timer in a low power state. The 4MHz RC timer is used as the MCU master timer and, when used in conjunction with the PLL, it can provide a timer up to 48MHz.

The 64k and 4M RC timers are factory calibrated, the 4M RC timer has a customized calibration register to further calibrate the accuracy to ±0.5%. In the temperature range of -40-105℃, the accuracy of the 64k RC timer is ±50% and that of the 4M RC timer is ±1%

The 64k RC timer frequency can be set with the register RCLTRIM <3:0>, and the 4M RC timer frequency can be set with the register RCHTRIM <5:0>, which corresponds to the values described in the analog register table.

The timer is calibrated before the chip is shipped from the factory, and generally, you do not need to configure these additional registers. To fine tune the frequency, you need to read the original configuration value and fill in the configuration value corresponding to the fine-tuning amount.

The 4M RC timer is turned on by setting RCHPD = '0' (on by default, and off when set to '1'). The RC timer requires the Bandgap voltage reference module to provide reference voltage and current. Therefore, it is necessary to enable the BGP module before turning on the RC timer. The 4M RC timer is turned on and the BGP module is enabled by default in case of chip power-up. The 64k RC timer is always turned on and cannot be turned off.

The PLL multiplies the frequency of the 4M RC timer, to ensure a higher-speed timer for modules such as MCU, ADC, etc. The highest timer of the MCU and PWM modules is 48MHz, while the typical timer of the ADC module is 24MHz.

The PLL module is enabled by setting PLLPDN = '1' (off by default, and on when set to 1). The BGP (Bandgap) module needs to be enabled before the PLL module. After enabling the PLL module, it will take a stabilization time of 6us to output a stable timer. By default when the chip is powered on, the RCH timer is turned on and the BGP module is enabled; however, the PLL module is disabled, and needs to be enabled with software.

9 Reference Voltage Source

The reference voltage source provides reference voltage and current for the ADC, DAC, RC timer, PLL, temperature sensor, operational amplifier, comparator, and FLASH. The reference voltage source of BGP needs to be enabled before using any of these modules.

The BGP module is enabled by default when the chip is powered on. The reference voltage source is enabled by setting BGPPD = '0', and BGP needs about 2us to stabilize from being enabled to disabled. The output voltage of BGP is about 1.2V with an accuracy of ±0.8%

10 ADC Module

A SAR ADC is integrated into the chip. The ADC module is disabled by default when the chip is powered on. Before the ADC is enabled, it is necessary to enable the BGP and PLL modules, turn on the 4M RC timer, and select the ADC operating frequency. The ADC operating timer is 24 M by default.

The ADC requires at least 17 ADC timer cycles to complete a conversion, of which 12 are conversion cycles and 5 are sampling ones. The sampling period can be set by configuring the SAMP_TIME register in SYS_AFE_REG2. It is required to set not less than 3 sampling periods, that is, more than 8 ADC clocks.

The recommended value is 3, which corresponds to an output data rate of 1.2MHz for the ADC.

The ADC operates in the following modes: single single-channel trigger, continuous single-channel trigger, single 1-16 channel scanning, and continuous 1-16 channel scanning. Each ADC has 16 independent sets of registers for each channel.

The ADC trigger event may come from external timer signals T0, T1, T2, T3 for a preset number of times, or may be triggered by software.

The ADC has two gain modes that are set by SYS_AFE_REG0.GA_AD, corresponding to 1 x time and 2/3 x times gains. The 1 x time gain corresponds to an input signal of ±2.4V, and the 2/3 x times gain corresponds to an input signal amplitude of ±3.6V. In measuring the output signal of an operational amplifier, the specific ADC gain is selected based on the maximum possible output signal of the operational amplifier.

11 Operational Amplifier

Two input and output rail-to-rail operational amplifiers, with a built-in feedback resistor R2/R1. External pins should be connected in series with a resistor R0. The value of resistance of the feedback resistors R2:R1 can be set via register RES_OPA <1:0> for different magnification. The values corresponding to the specific registers are described in the analog register table.

The final magnification is R2/(R1+R0), where R0 is the value of resistance of the external resistor.

A capacitor greater than or equal to 15pF is required to be connected across the two input pins of the op amp.

For applications of direct sampling of MOS transistor resistor, it is recommended to connect an external resistor of >20kΩ to reduce the current flowing into the chip pins when the MOS transistor is turned off.

For small resistor sampling applications, external resistors of 100Ω are recommended.

The amplifier can select the output signal in the amplifier by setting OPAOUT_EN to send it to P0.7 IO port through BUFFER for measurement and application. Because BUFFER exists, it is also possible to send one output signal of the op amp under its normal operation mode.

In the default state when the chip is powered up, the amplifier module is turned off. The amplifier can be enabled by setting OPAPDN = '1' and the BGP module should be enabled before enabling the amplifier.

The clamping diode is built into the positive and negative input terminals of the op amp, and the motor phase line is directly connected to the input terminal through a matching resistor, thus simplifying the external circuit of MOSFET current sampling.

12 Comparator

There is a built-in 2 comparators, of which the comparison speed, the hysteresis voltage, and the signal source are programmable.

The comparator has a comparison delay of 0.15us and can also be set to less than 30ns via register CMP_FT. The hysteresis voltage is set to 20mV/0mV via CMP_HYS.

The signal source for both the positive and the negative inputs of the comparator can be programmed through the registers CMP_SELP<2:0> and CMP_SELN<1:0> as described in the register simulation instructions.

The comparator module is turned off by default when the chip is powered on. The comparator can be enabled by setting CMPxPDN ='1' and the BGP module should be enabled before enabling the comparator.

13 Temperature Sensor

A temperature sensor with an accuracy of ±2℃ is built into the chip. The chip will undergo temperature correction before delivery, and the correction value is saved in the flash info area.

The temperature sensor module is turned off by default when the chip is powered on. The BGP module should be enabled before enabling the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1'. It takes approximately 2us to turn on until stable, so it needs to be turned on 2us before the ADC measures the sensor.

14 DAC Module

The chip has A built-in 8-bit DAC, and the output signal range of the A version is 3V, the output signal range of the B version is 3V/4.8V, and the output signal range of the C version is 1.2V/3V/4.8V.

For the C version of the chip, you need to set SYS AFE REG2.BIT15=1 to use the DAC's 1.2V range.

The 8bit DAC can be configured with register DACOUT EN=1 to send the DAC output to the IO port P0.0, which can drive a load resistance >50kΩ and a load capacitor of 50pF.

Since 03x series chips are not equipped with DAC hardware correction registers, in order to ensure DAC output accuracy, users need to read DACAMC/DACDC correction values of corresponding ranges from NVR according to different DAC ranges for software correction.

The digital quantity corresponding to the expected output value of the DAC is D_{DAC}, the gain correction is DAC_{AMC}, and the DC bias correction is DAC_{DC}. The DAC_{AMC} is a 10bit unsigned number, the $DAC_{AMC}[9]$ is an integer part, and the $DAC_{AMC}[8:0]$ is a decimal part, which can represent a fixed-point number near 1, and 0x200 corresponds to 1. The Saturation values are as follows:

SYS_AFE_DAC = Saturation(D_{DAC}*DAC_{AMC}-DAC_{DC})

See the official library function for details.

The maximum output bit rate of the DAC is 1MHz.

When the chip is powered on, the DAC module is disabled by default. The DAC can be enabled by setting DACPDN =1. Before enabling the DAC module, enable the BGP module.

15 Processor

- 32-bit Cortex-M0 +DIV/SQRT coprocessor
- 2-wire SWD debugging pin
- Maximum operating frequency: 48MHz

16 Storage Resources

16.1 Flash

- The built-in flash includes a main storage area of 16/32kB and an information storage area of 1kB NVR
- Repeatable erasing and write-in of not less than 20,000 times
- Data is maintained for up to 100 years at a room temperature of 25℃
- The single-byte programming time is up to 7.5us, and the Sector erasing time is up to 5ms
- The Sector is 512 bytes, and can be erased or write-in by Sector. It supports runtime programming
- Flash data anti-theft (the last word must be written to any value other than 0xFFFFFFFF)

16.2 Execute-only Zone

Some 16kB flash capacity models are equipped with an execute-only zone of 16kB. After programming encryption, such models have the execution permission but do not have the read or write permission. Reprogramming with repeated erasure is supported.

16.3 SRAM

- Built-in 4KB SRAM

17 MCPWM Dedicated to Motor Drive

- The maximum operating timer frequency of MCPWM is 48MHz
- Supporting up to 4 channels complementary PWM outputs with adjustable phases
- The dead zone width of each channel can be configured independently
- Edge-aligned PWM mode supported
- Software control IO mode supported
- IO polarity control supported
- Internal short-circuit protection: avoiding short circuits caused by incorrect configuration
- External short-circuit protection: fast shutdown based on monitoring of external signals
- ADC sampling interrupt generates internally
- Use load register pre-memory timer to configure parameters
- The loading time and period of the loading register can be configured

18 Timer

- Two general-purpose timers, one 16bit timer and one 32bit timer
- Capturing mode is supported for measuring external signal width
- Comparison mode is supported for generating edge-aligned PWM/timing interrupts

19 Hall Sensor Interface

- Built-in maximum 1024 filtering
- Three Hall signal input
- 24-bit counter with overflow and capture interrupts

20 General Purpose Peripherals

- One UART works in the full-duplex operation mode, supporting 8/9 bits of data, 1/2 stop bit(s), odd/even/no parity mode, with 1 byte send cache, 1 byte receive cache, with Multi-drop Slave/Master mode, and the baud rate ranging from 300-115200
- One SPI for master-slave mode
- One IIC for master-slave mode
- Hardware watchdog, driven by RC timer, being independent of system high speed timer, write-in protection

21 Gate Drive Module

21.1 Module Parameters

The internal gate drive module of the chip has six different parameter specifications. According to the different parameters of the gate drive circuit, the gate drive module is divided into six models, namely G2, G3, G5, G6, G7 and G8. The comparison table is shown in Table 22-1.

Table 21-1 Comparison Table of Chip Models and Gate Drive Circuits

MCU	Model of gate drive module
LKS32MC031KLC6T8B/C	G7
LKS32MC034DF6Q8(B/C)	G2
LKS32MC034DOF6Q8(B/C)	G2
LKS32MC034FLF6Q8B/C	G6
LKS32MC034FLK6Q8C	G6
LKS32MC034SF6Q8(B/C)	G3
LKS32MC034S2F6Q8B/C	G6
LKS32MC038KU6Q8B	G5
LKS32MC034F2LF6Q8C	G8
LKS32MC034F2LM6Q8C	G8
LKS32MC034FLNK6Q8C	G6
LKS32MC034F2LNK6Q8C	G8

21.1.1 Gate Drive Module G7

Table 21-2 Parameter of Gate Drive Module G7

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+25.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	-0.3		+650	V	
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input HIN/$LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+13		+20.0	V	Relative to ground

Floating voltage $VB_{1,2,3}$	VS+13		VS+20	V	
Floating bias $VS_{1,2,3}$	-5		600	V	
High-side output voltage $HO_{1,2,3}$	VS		VB	V	
Low-side output voltage $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	
Operating temperature T_A	-40		105	°C	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC}			2300	uA	HIN=LIN=0V
VB static current I_{QBS}			100	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			50	uA	VB=VS=620V
VCC supply under-voltage trigger voltage	11	12	12.8	V	
VCC supply under-voltage lock -on voltage	9.5	10.4	11	V	
VCC supply under-voltage hysteresis voltage	1	1.6	2	V	
High input threshold V_{IH}	1.7		2.4	V	
Low input threshold V_{IL}	0.8	1.0	1.2	V	
High level output short current I_{O+}	115	200		mA	
Low level output short current I_{O-}	250	350		mA	
Short circuit trip level V_{CIN_REF}	0.455	0.48	0.505	V	VCC=15V
Fault output voltage V_{FOL}			0.95	V	
Fault output pulse width t_{FO}	20	65		us	
Output rise time T_r		65		ns	C_L=1nF
Output fall time T_f		25		ns	
Turn-on delay time T_{on}	350	500	700	ns	
Shutdown delay time T_{off}	350	500	700	ns	
Delay matching M_T			60	ns	T_{on} & T_{off} for (HS-LS)
CIN detection input filter time $T_{FLT-CIN}$	100	300	500	ns	CIN 0->1V, test CIN rising edge to LO falling edge delay

21.1.2 Gate Drive Module G2

Table 21-3 Parameter of Gate Drive Module G2

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+25.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	-0.3		+250	V	
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	

Logic input HIN/LIN1, 2, 3	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+8		+20.0	V	Relative to ground
Floating voltage VB1, 2, 3	VS+8		VS+20	V	
Floating bias VS1, 2, 3	-5		200	V	
High-side output voltage HO1, 2, 3	VS		VB	V	
Low-side output voltage LO1, 2, 3	0		VCC	V	
Logic input HIN/LIN1, 2, 3	0		VCC	V	
Operating temperature T_A	-40		105	℃	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC}		50	100	uA	HIN=LIN=0V
VB static current I_{QBS}		20	40	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			10	uA	VB=VS=220V
VCC supply under-voltage trigger voltage	4.0	4.7	6.7	V	
VBS supply under-voltage trigger voltage	3.9	5.6	6.9	V	
VCC supply under-voltage lock -on voltage	3.6	4.4	6.4	V	
VBS supply under-voltage lock -on voltage	3.5	5.0	6.2	V	
VCC supply under-voltage hysteresis voltage	0.25	0.3	0.8	V	
VBS supply under-voltage hysteresis voltage	0.25	0.6	0.8	V	
High input threshold V_{IH}	2.8			V	
Low input threshold V_{IL}			0.8	V	
Input bias current I_{source}		50	120	uA	HIN=LIN=5V
Input bias current I_{sink}			1	uA	HIN=LIN=0V
High level output, V_{BIAS}-V_O			1	V	I_O=20mA
Low level output, V_O			1	V	I_O=20mA
High level output short current I_{O+}	650	1000		mA	V_{CC}/V_{BS}=15V
Low level output short current I_{O-}	650	1000		mA	V_{CC}/V_{BS}=15V
Output rise time T_r		15	30	ns	C_L=1nF
Output fall time T_f		12	30	ns	
Turn-on delay time T_{on}		270	500	ns	
Shutdown delay time T_{off}		80	150	ns	
Dead zone D_T	100	200	400	ns	

Delay matching M_T			80	ns	T_{on} & T_{off} for (HS-LS)

21.1.3 Gate Drive Module G3

Table 21-4 Parameter of Gate Drive Module G3

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+25.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	-0.3		+250	V	
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+7		+20.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	VS+10		VS+20	V	
Floating bias $VS_{1,2,3}$	-5		200	V	
High-side output voltage $HO_{1,2,3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low-side output voltage $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		5	V	
Operating temperature T_A	-40		105	℃	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC1}	210	330	450	uA	HIN=LIN=0/5V, ENB=0
VCC static current I_{QCC2}		46	80	uA	HIN=LIN=0/5V, ENB=5
VB static current I_{QBS}	25	45	65	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			10	uA	VB=VS=200V, VCC=0V
drive current I_{O+}		1		A	
drive current I_{O-}		1.2		A	
VCC undervoltage rising edge trigger voltage	2.9	4.2	5.5	V	
VCC undervoltage falling edge trigger voltage	2.5	3.8	5.1	V	
VCC undervoltage lockout hysteresis		0.4		V	

VBS undervoltage rising edge trigger voltage	2.5	3.8	4.5	V	
VBS undervoltage falling edge trigger voltage	2.5	3.5	4.5	V	
VBS undervoltage lockout hysteresis		0.3		V	
High input threshold V_{IH}	2.5			V	
Low input threshold V_{IL}			0.8	V	
Output rise time T_r		27		ns	C_L=1nF
Output fall time T_f		20		ns	
Turn-on delay time T_{on}		600	700	ns	
Shutdown delay time T_{off}		280	400	ns	
Dead zone D_T	220	280	330	ns	
Delay matching M_T			60	ns	

21.1.4 Gate Drive Module G5

Table 21-4 Gate Drive Module G5 parameter

Parameter	Min	Typ	Max	Unit	Description
Absolute Maximum Ratings					
Low side and logic fixed supply VCC	-0.3		+25.0	V	To ground
High side floating supply VB	-0.3		+625	V	
High side offset VS	VB-25		VB+0.3	V	
High side output $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low side output $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Allowable offset voltage slew rate dVs/dt			50	V/ns	
Junction temperature TJ	-40		150	℃	
Storage temperature Ts	-55		150	℃	
Thermal resistance θJA			200	℃/W	junction to ambient
Recommended Operating Conditions					
Low side and logic fixed supply VCC	+10		+20.0	V	To ground
High side floating supply VB	VS+10		VS+20	V	
High side offset VS	-5		600	V	
High side output $HO_{1,2,3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low side output $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	

Operating temperature T_A	-40		105	℃	
Gate driver Electrical Characteristic					
Quiescent VCC supply currentI_{QCC}		50	150	uA	HIN=LIN=0V
Quiescent VBS supply currentI_{QBS}		35	80	uA	HIN=LIN=0V
Offset supply leakage currentI_{LK}			10	uA	VHO=VB=VS=620V
VCC under voltage rising threshold	8	8.5	9.8	V	
VBS under voltage rising threshold		8.7	10	V	
VCC under voltage falling threshold	7.2	7.6	8.8	V	
VBS under voltage falling threshold	6.5	7.8		V	
VCC under voltage hysteresis voltage	0.6	0.9	1.2	V	
VBSunder voltage hysteresis voltage		0.9		V	
High level output voltage V_{IH}	2.4			V	
Low level output voltage V_{IL}			0.6	V	
Logic 1 Input bias current I_{source}		32	100	uA	HIN=LIN=5V
Logic 0 Input bias current I_{sink}			1	uA	HIN=LIN=0V
High level output voltage V_{OH}			1	V	I_O=20mA
Low level output voltage, V_{OL}			1	V	I_O=20mA VO=0V, VIN=5V,Pulse Width < 10uS
Output high short circuit pulse current I_{O+}	300	450		mA	
Output low short circuit pulse current I_{O-}	650	1000		mA	VO=15V, VIN=0V,Pulse Width < 10uS
Turn-on rise time T_r		15	30	ns	C_L=1nF
Turn-off fall time T_f		12	30	ns	
Turn-on propagation delay T_{on}	100	250	450	ns	VS=0V
Turn-off fall time T_{off}	80	160	300	ns	VS=0V or 600V
Dead time D_T	40	100	250	ns	

Delay match M_T			80	ns	T_{on} & T_{off} for (HS-LS)

Ensure that the time Δt for the high-side MOS Vgs to rise to VS is < 300 ns:

- Select the appropriate drive circuit and adjust Ron and Cgs appropriately;
- Pay attention to the turn-on voltage of MOS/IGBT. If Vth is higher, it is more important to ensure that the rise time of Vgs is short enough.

21.1.5 Gate Drive Module G6

Table 21-5 Parameter of Gate Drive Module G6

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+22.0	V	Relative to ground
Floating voltage $VB_{1, 2, 3}$	-0.3		+250 +60	V	VEM is not used for 034S2F6Q8B, the with-stand voltage is 250 V, and the rest is 60 V. VSx and VSSNx are internally shorted, and if the maximum VSx voltage exceeds 60 V, a parallel resistor from VEMx to ground is re-quired to reduce the voltage division ratio.
Floating bias $VS_{1, 2, 3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1, 2, 3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1, 2, 3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1, 2, 3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+7.0		+20.0	V	Relative to ground
Floating voltage $VB_{1, 2, 3}$	VS+8		VS+20	V	
Floating bias $VS_{1, 2, 3}$	-5		60	V	034S2 $VS_{1, 2, 3Max}$=200V
High-side output voltage $HO_{1, 2, 3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low-side output voltage $LO_{1, 2, 3}$	0		VCC	V	

Logic input HIN/LIN$_{1,2,3}$	0		5	V	
Operating temperature T_A	-40		105	°C	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC}		110		uA	HIN=LIN=0/5V
VB static current I_{QBS}		25	50	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			10	uA	VB=VS=200V, VCC=0V
drive current I_{O+}	0.65	1		A	
drive current I_{O-}	0.65	1		A	
VCC undervoltage rising edge trigger voltage	3.5	4.2	4.9	V	
VCC undervoltage falling edge trigger voltage	3.2	3.8	4.8	V	
VCC undervoltage lockout hysteresis	0.25	0.4	0.8	V	
VBS undervoltage rising edge trigger voltage	2.5	3.8	5.5	V	
VBS undervoltage falling edge trigger voltage	2.2	3.5	4.8	V	
VBS undervoltage lockout hysteresis	0.25	0.3	0.8	V	
High input threshold V_{IH}	2.8			V	
Low input threshold V_{IL}			0.8	V	
Output rise time T_r		20	30	ns	C_L=1nF
Output fall time T_f		12	30	ns	
Turn-on delay time T_{on}		250	500	ns	
Shutdown delay time T_{off}		120	200	ns	
Dead zone D_T	50	150	400	ns	
Delay matching M_T			80	ns	
LDO linear adjustment parameter					
LDO Output Voltage V_{LDO}	4.8	5.0	5.2	V	The factory test records the 5V LDO voltage in the flash area for the software to read.Refer to the data sheet for the address of the Flash NVR correction values
LDO output with load current I_{LDO}		30		mA	
Load regulation	-0.297		+0.397	%	Load current 0~35mA
Linear adjustment rate		0		%	VCC from 7-22V
Short circuit current	122		142	mA	

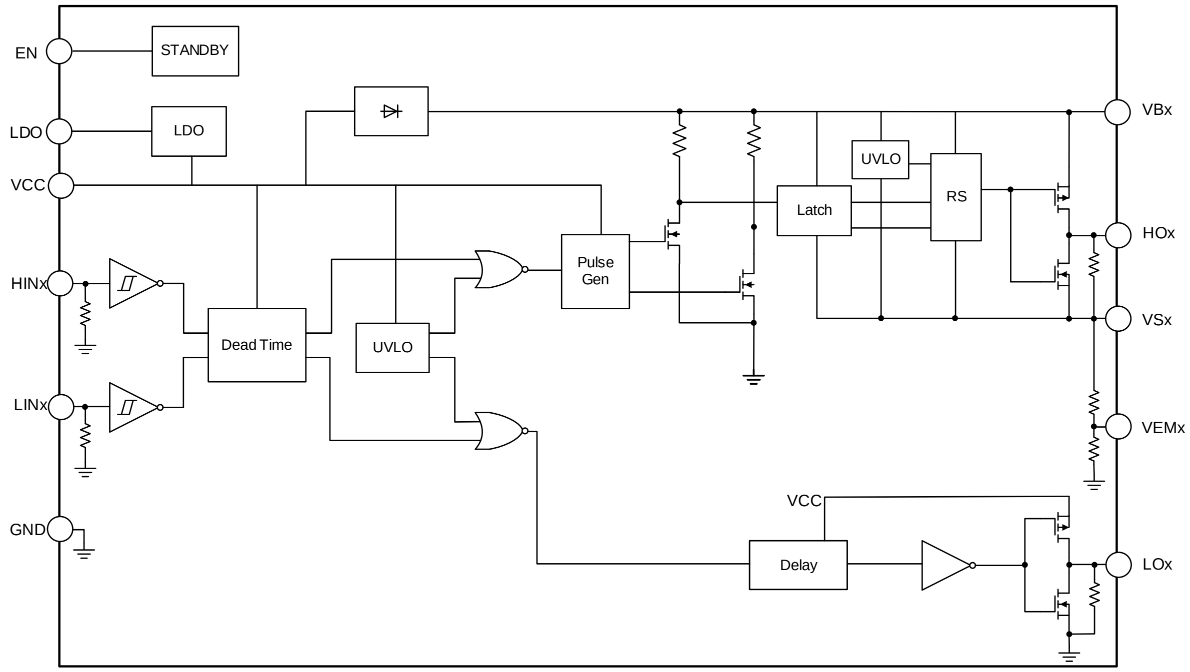

Figure 21-1 Internal block diagram of gate drive module G6

21.1.6 Gate Drive Module G8

表 21-1 栅极驱动模块参数

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage V_{CC}	-0.3		+48.0	V	Relative to the ground
Charge Pump Supply Voltage V_M	-0.3		V_{CC}	V	
Charge pump high voltage pin CP V_{CP}	-0.3		V_{CC}+20		
Charge pump high voltage pin CN V_{CN}	-0.3		V_{CC}		
Floating voltage $VB_{1,2,3}$	-0.3		+90	V	
Floating bias $VS_{1,2,3}$	-0.3		V_{CC}+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		+20	V	
Counter electromotive force voltage sampling input pin V_{SSN}	-0.3		V_{CC}+0.3	V	
V_{LDO}	-0.3		+6	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		+6	V	
Switching slew rate dVs/dt	-		50	V/ns	
Analog Output Voltage $(V_{bus}/VEMx)V_{OUT}$	-0.3		+6	V	
Power-down holds the external interface $V_{K\text{-}Ctrl}$	-0.3		V_{CC}	V	

External interface of double-plug switch V_{EXT}	-0.3		V_{CC}	V	
Junction temperature TJ	-40		150	°C	
Storage temperature Ts	-55		150	°C	
Welding temperature			300	°C	Weld for 10 s
Recommended operating conditions (T_A = 25℃)					
Supply voltage V_{CC}	-0.3		+40.0	V	Relative to the ground
Charge Pump Supply Voltage V_M	-0.3		V_{CC}	V	
Floating voltage $VB_{1,2,3}$	V_M+10		V_M+15	V	
Floating bias $VS_{1,2,3}$	-5		+80	V	
Logic Input Voltage (PWMx/M_Ctrl/D_Ctrl)	0		+5	V	
Analog Output Voltage V_{OUT}	0		+5	V	Vbus/VEMx
Electrical parameters (Unless otherwise specified,V_{CC} = V_M = 24V, T_A = 25℃)					
Supply voltage					
Power-on turn-on voltage V_{CC_ON}	3.9	4.2	4.5	V	
Undervoltage lockout voltage V_{CC_OFF}	3.6	3.9	4.2	V	
Undervoltage protection hysteresis voltage V_{CC_HYS}	-	0.3	-	V	
Quiescent current I_{QCC}	-	850	-	uA	PWM=0, MCU not included
Standby current I_{STBY}	-	-	10	uA	M_Ctrl=0/K_Ctrl=0 , Not enabled
Charge pump					
Charge Pump Output Voltage V_{CP}	-	12	-	V	VB-VM
Charge pump load current I_{CP}	-	15	-	mA	PWM switching frequency 20kHz to meet output voltage require-ment
Charge Pump Output Current Limit I_{CP_LIM}	30	40	-	mA	
V_{CP} Undervoltage release point V_{CP_ON}	3.6	3.9	4.2	V	
V_{CP} Undervoltage protection point V_{CP_OFF}	3.3	3.6	3.9	V	
V_{CP} Undervoltage hysteresis V_{CP_HYS}	-	0.3	-	V	
Charge pump ripple voltage ΔVCP		300		mV	
5V LDO					
LDO Output voltage V_{LDO}	4.8	5.0	5.1	V	
V_{DROP}		0.2		V	VM=5V, I_{LDO}=10mA

LDO Load current I_{LDO}	50			mA	Meets output voltage requirement
LDO Output current limit value I_{LDO_LIM}		200		mA	
V_{LDO} Undervoltage release point V_{LDO_ON}		3.3		V	
V_{LDO} Undervoltage protection point V_{LDO_OFF}		3		V	
V_{LDO} Undervoltage hysteresis V_{LDO_HYS}		0.3		V	
Linear adjustment rate			50	mV	
Load regulation			50	mV	
Power supply rejection ratio	50	60		dB	1kHz
Digital IO features V_{AVDD}=5V					
Digital IO Input High Voltage V_{IH}		1.7	2	V	
Digital IO Input Low Voltage V_{IL}	0.65	1.2		V	
Digital IO Input Pull-Down Resistor R_{PD}	-	100		kΩ	
Schmidt hysteresis range V_{HYS}	-	0.5	-	V	
Digital IO input high voltage, current consumption I_{IH}	-	-	100	uA	V_{IN}=5V
Digital IO input low voltage, current consumption I_{IL}	-	-	1	uA	V_{IN}=5V
Analog IO characteristics					
K_Ctrl Input high voltage V_{K_CtrlH}		2.7		V	
K_Ctrl Input low voltage V_{K_CtrlL}		2.4		V	
K_Ctrl Active level hysteresis voltage $V_{K\_Ctrl\_HYS}$		0.3		V	
K_Ctrl Input pull-down resistor $R_{K\_Ctrl\_PD}$		200		kΩ	
EXT Enable impedance to ground R_{EXT_ON}			1	kΩ	
EXT Do not enable ground leakage R_{EXT_OFF}	5			kΩ	
Gate driver					
V_{OH}	-	-	1	V	I_O=20mA
V_{OL}	-	-	1	V	I_O=20mA
I_{O+} 000b		1000		mA	High level output short circuit pulse current, short circuit pulse width < 10 us
001b		400			
010b		300			
011b		200			
100b		150			
101b		125			
110b		100			

	111b		75			
I_{O-}	000b		1000		mA	Low level output short circuit pulse current, short circuit pulse width < 10 us
	001b		400			
	010b		300			
	011b		200			
	100b		150			
	101b		125			
	110b		100			
	111b		75			
Bus voltage detection						
V_M Detect pull-up resistor R_{Vbus_PU}		106			kΩ	
V_M Detect pull-down resistor R_{Vbus_PD}		6.8			kΩ	
V_M Partial voltage output ratio R_{Vbus}		16			V/V	V_{bus}/V_M
Back EMF voltage detection						
Detect pull-up resistor R_{VEM_PU}		38			kΩ	
VEM Detect the pull-down resistor R_{VEM_PD}		3.5			kΩ	Option 1
		9.5			kΩ	Option 2
VSSN Partial voltage output ratio R_{VSSN}		12			V/V	VEM/VSSN option 1
		5			V/V	VEM/VSSN option 2
VEM Detect the pull-down capacitance C_{VEM_PD}		10			pF	
Dynamic electrical parameters C_L=1nF						
High side on propagation delay T_{ON_HS}	-	250	500		ns	V_S=0V
Low side on propagation delay T_{ON_LS}	-	250	500		ns	
High side off propagation delay T_{OFF_HS}	-	120	200		ns	V_S=0V or 40V
Low side off propagation delay T_{OFF_LS}	-	120	200		ns	
Output rise time T_r	-	20	30		ns	IO+=1A
Output fall time T_f	-	12	30		ns	IO-=1A
Dead time DT	50	130	400		ns	
Matching of high and low measurement transmission delay MT	-	-	80		ns	T_{ON} & T_{off} for (HS-LS)
Time sequence						
VCC Power-Up to LDO Voltage Setup Time T_{LDO_ready}		TBD			us	
VCC Power-Up to Gate driver Output Setup Time T_{SW_ready}			2		ms	
Short circuit protection						
Short circuit protection shielding time T_{SCP_Blank}	1.2	2.0	2.8		us	
Down tube short circuit threshold		2.1			V	

Upper tube short circuit threshold		1.9		V	
Over-temperature protection					
Over-temperature protection threshold T_{OTP}	165	175	185	℃	
Over-temperature protection release point T_{OTP_Rel}	135	145	155	℃	

OWSI interface

The LKS69231 communicates with the MCU via the OWSI interface (D _ Ctrl pin).The LKS69231 incorporates the following registers to calibrate or set the internal blocks and return status information.

Type/Register Name	Address	Explain
Ctrl	7' H15~7' H0E	7' H0E: High and low side short circuit protection cancel bit, default 0, write 1 cancel 7' H0F: Back-EMF sampling ratio selection bit, default 0, ratio 12:1, write 1, ratio 5:1 7' H12~7' H10: HS/LS IO+ drive capability selection bit, refer to I_{o+} information of Gate driver part in electrical parameters for specific meaning 7' H15~7' H13: HS/LS IO- drive capability selection bit, refer to I_{o-} information of Gate driver part in electrical parameters for specific meaning
Status	7' H27~7' H1D	The default state is 0, and a state of 1 indicates that protection is triggered 7' H1F~7' H1D: Short-circuit signal of phase u, V and w low-side power tube, write 1 to clear 7' H22~7' H21: U, V, w phase high side power tube short circuit signal, write 1 to clear 7' H23: otp 7' H24: vcp_ok 7' H25: vm_uvlo 7' H26: vdd_uvlo 7' H27: not_ready_flag, 0 for ready, 1 for not ready

21.2 Recommended Application Diagram

The output pin signal LO1/HO1 of the driver module corresponds to the MCPWM function output of GPIO P0.10/P0.13, LO2/HO2 corresponds to the MCPWM function output of GPIO P0.11/P0.14, and LO3/HO3 corresponds to the MCPWM function output of GPIO P0.12/P0.15.

The MCPWM_SWAP register must be set for the integrated pre-drive chip, otherwise the PWM cannot be output normally. Write 0x67 to such register to write BIT[0] to 1, and write other values to write BIT[0] to 0. When the value of MCPWM_SWAP is 1, it is used to include the pre-drive chip application environment. The sequence is converted within the logic to facilitate the interconnection of the chip and the drive chip. In general applications, only three sets of MCPWM channels are required, so only three sets of sequences are converted.

21.2.1 Gate Drive Module G7

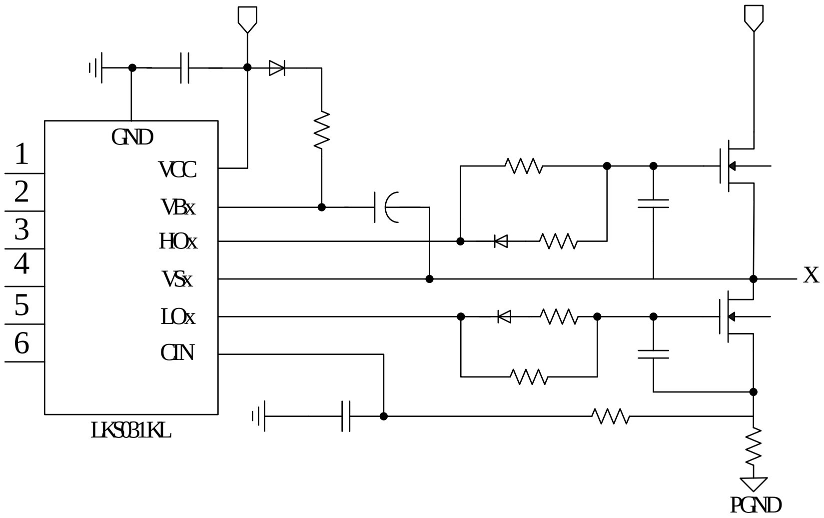

Figure 21-2 Typical Application Diagram of 6N Type Gate Drive Module LKS32MC031KLC6T8B

21.2.2 Gate Drive Module G5

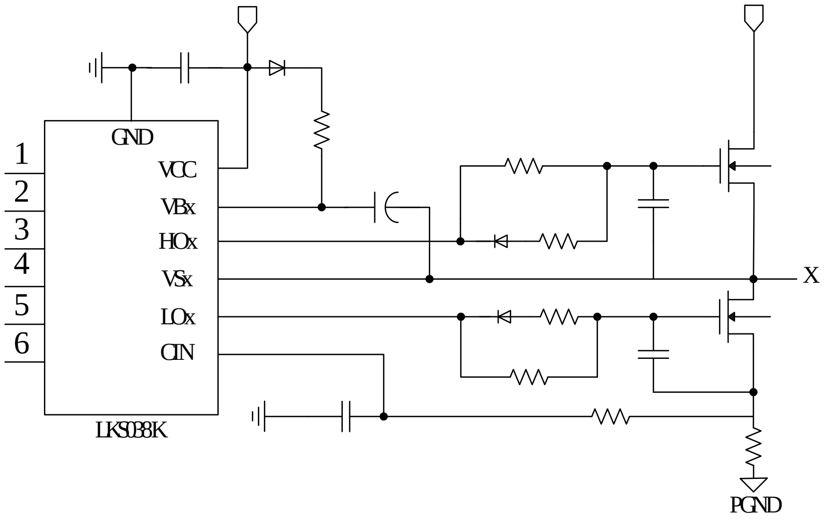

Figure 21-3 Typical Application Diagram of 6N Type Gate Drive Module LKS32MC038KU6Q8B

21.2.3 Gate Drive Module G2

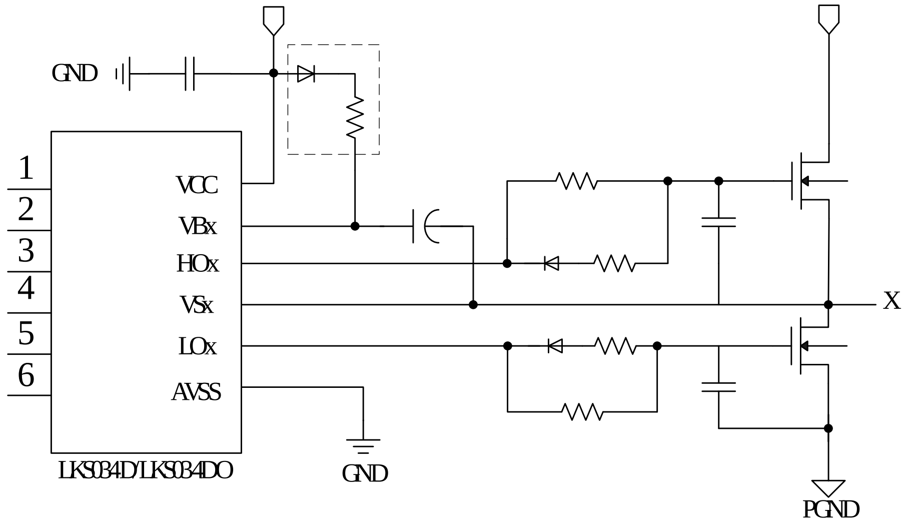

Figure 21-4 Typical Application Diagram of 6N Type Gate Drive Module LKS32MC034D(O)F6Q8

21.2.4 Gate Drive Module G6

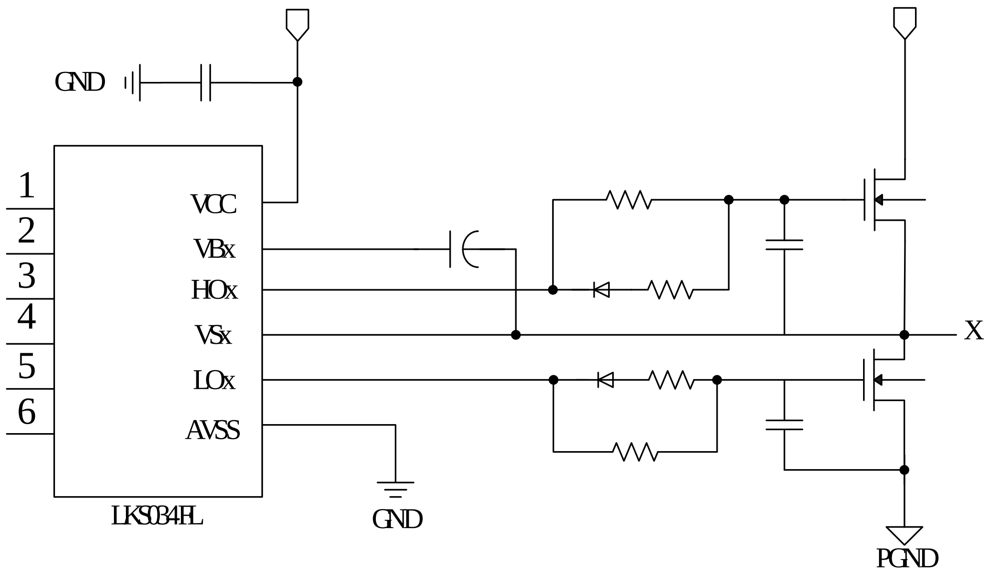

Figure 21-4 Typical Application Diagram of 6N Type Gate Drive Module LKS034FL

21.2.5 Gate Drive Module G3

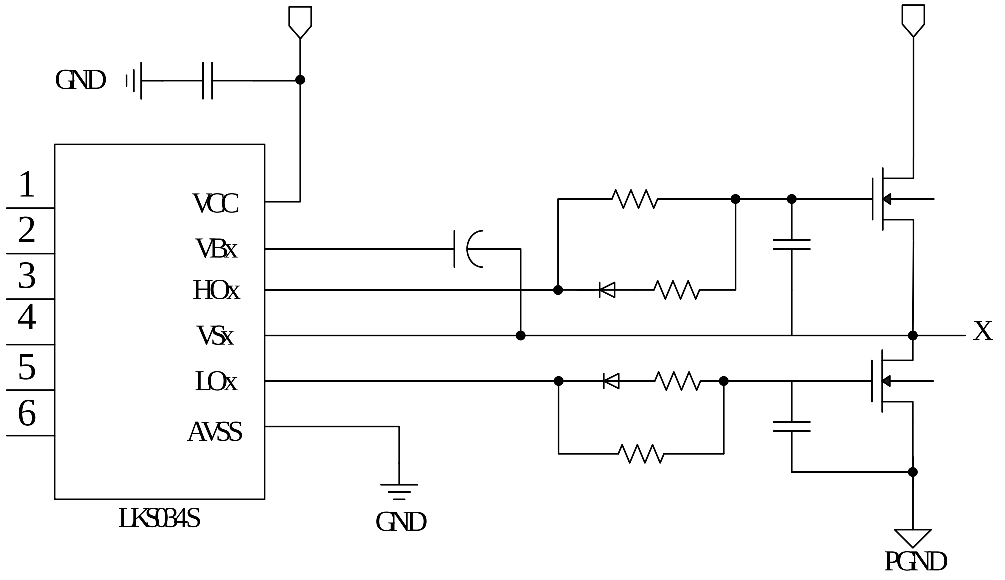

Figure 21-5 Typical Application Diagram of 6N Type Gate Drive Module LKS034S

In the figure, only the pins of the gate drive module are retained, x=1, 2, 3, corresponding to 3 groups of MOS gate drive outputs respectively. The application diagram for each group is shown above.

Each GPIO controlling the LOx of the drive module is a high level '1' corresponding to the LOx output '1'.

The input/output polarity of gate drive module is as follows:

Table 21-3 LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Gate Drive Polarity Truth Table

{HIN, LIN}	HO	LO	
00	0	0	Shutdown of upper and lower tubes
01	0	1	Lower tube conduction
10	1	0	Upper tube conduction
11	0	0	The upper and lower tubes are connected simultaneously, and the hardware is under short-circuit protection

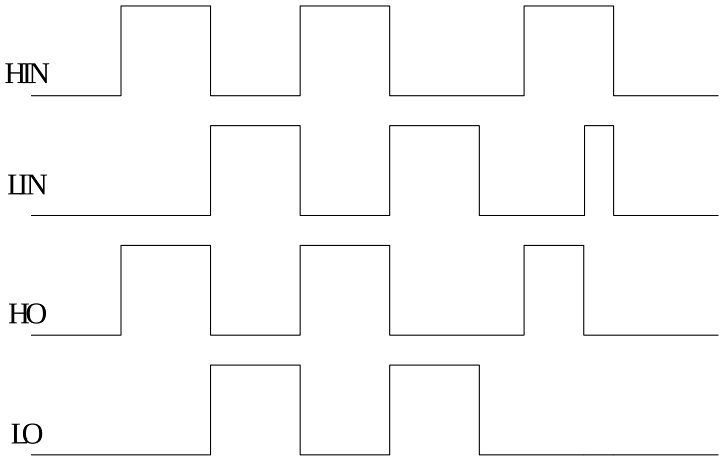

Figure 21-6 Schematic Diagram of LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Gate Drive Polarity

21.2.6 Gate Drive Module G8

The output pin signal LO1/HO1 of the drive module corresponds to the MCPWM function output of GPIO P0.10/P0.13, LO2/HO2 corresponds to the MCPWM function output of GPIO P0.11/P0.14, and LO3/HO3 corresponds to the mcpwm function output of gpio P0.12/P0.15.

The chip with integrated pre-driver needs to set the MCPWM _ SWAP register, otherwise the PWM cannot be output normally.Writing 0x67 to this register sets BIT [0] to 1. Writing any other value sets BIT [0] to 0.When the value of the MCP WM _ SWAP is 1, it is used for the application environment containing the pre-driver chip.The sequence is converted within the logic to facilitate the interconnection between the chip and the driver chip. In general, only three groups of MCPWM channels are required, so only three groups of sequences are converted.

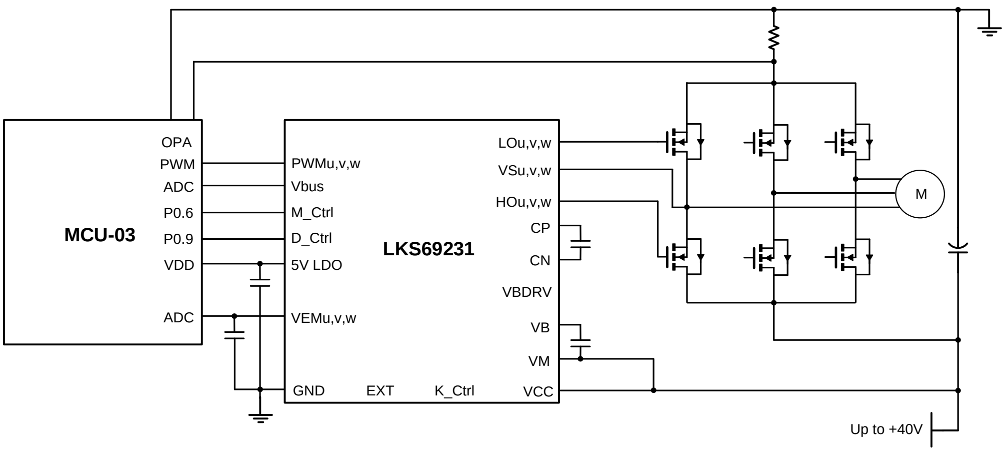

Figure 21-5 Typical application diagram of gate drive module

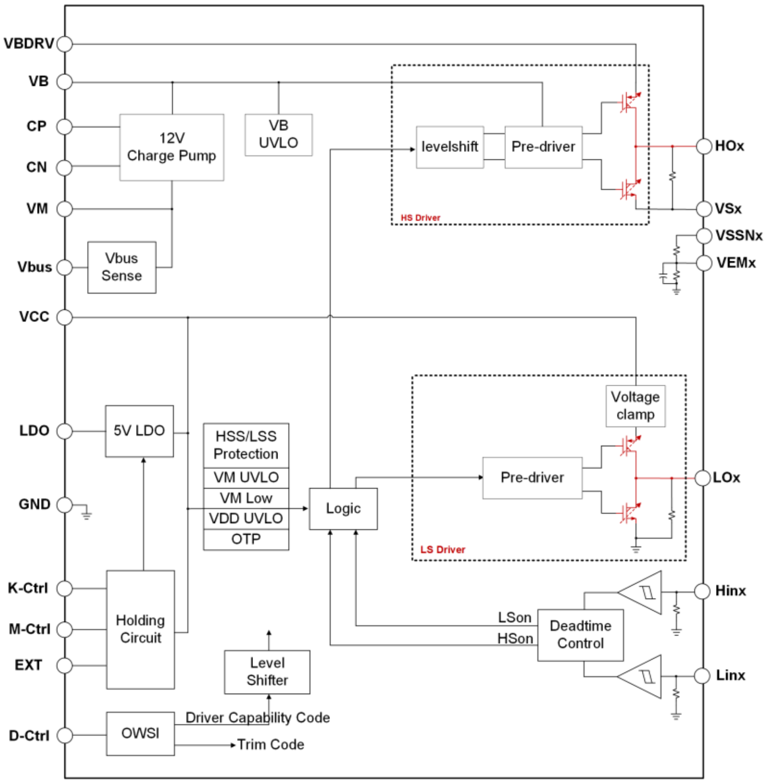

Figure 21-2 6 N-type gate drive module block diagram

The corresponding relationship between the input and output polarities of the grid drive module is as follows:

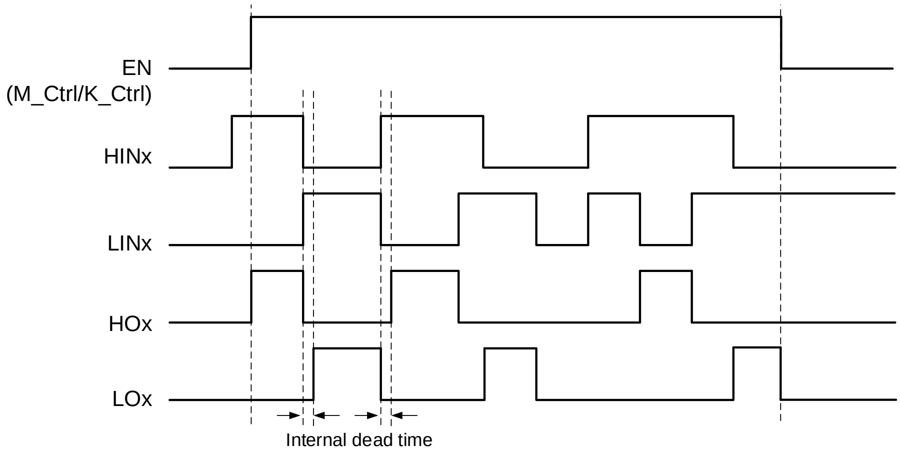

Figure 21-3 6 N-Type Gate Drive Polarity Diagram

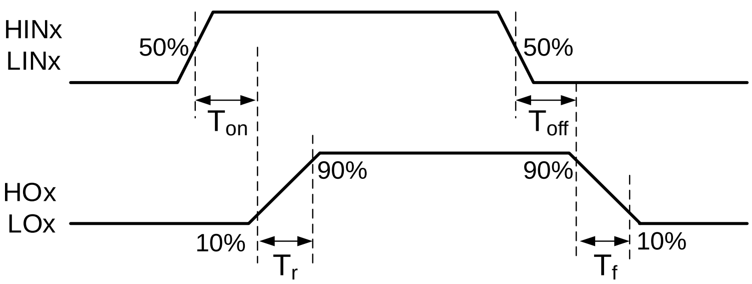

Figure 20-4 Switching sequence

22 DCDC Converter

LKS32MC034FLNK and LKS32MC034F2LNK include DCDC converter

22.1 Asynchronous Step-down DCDC Converter Parameter

Table 22-1 DCDC Converter Parameter

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
V_{IN}	-0.3		+105.0	V	Relative to the ground
BST	-0.3		+110.0	V	
SW	-1		105	V	
BST-SW	-0.3		5.5	V	
FB	-0.3		5.5	V	
Junction temperature T_J	-40		150	°C	
Storage temperature T_{STG}	-65		150	°C	
Recommended operating conditions					
V_{IN}	5.5		100	V	
V_{OUT}	1.2		30	V	
T_J	-40		150	°C	
ESD					
V_{ESD}	-2		2	kV	Human body model.（HBM）, AN-SI-JEDEC-JS-001-2014 compliant, all pin
	-1		1	kV	Charging Device Model (CDM) per AN-SI-JEDEC-JS-002-2014, All Pin
Electrical parameters					
Supply voltage					
V_{IN}	5.5		100	V	
V_{UVLO}	4.55	5	5.45	V	V_{IN} rising
		420		mV	Hysteresis
I_{SHDN}		4.3	8	uA	
			10	uA	T_J=-40°C~125°C
I_Q	30	49	65	uA	no load, non- switching,
	20		80	uA	T_J=-40°C~125°C
I_A		68		uA	V_{OUT}=12V
Power MOSFET					

R_{DSON_H}	600	975	1700	mΩ	V_{BOOT}-V_{SW}=5V
Reference control voltage					
V_{REF}	1.17	1.2	1.23	V	Tj=25°C
	1.16		1.24	V	Tj=-40°C~125°C
Soft start					
T_{SS}		3.5		ms	
Switching frequency					
F_{SW}	200	270	340	kHz	
T_{OFF_MIN}		250		ns	
Current display and overcurrent protection					
I_{LIM}	1.25	1.8	2.5	A	V_{IN}<60V
	0.95	1.5	2.2	A	V_{IN}≥60V
T_hiccup		7		SS cy-cles	
Protect					
V_{OVP}		120		%	V_{FB}/ V_{REF} rising
		115		%	V_{FB} / V_{REF} falling
V_{UVP}		45		%	V_{FB} / V_{REF} rising
		40		%	V_{FB} /V_{REF} falling
T_{SD}		155		℃	T_J rising
		13		℃	Hysteresis

22.2 Internal Functional Block Diagram

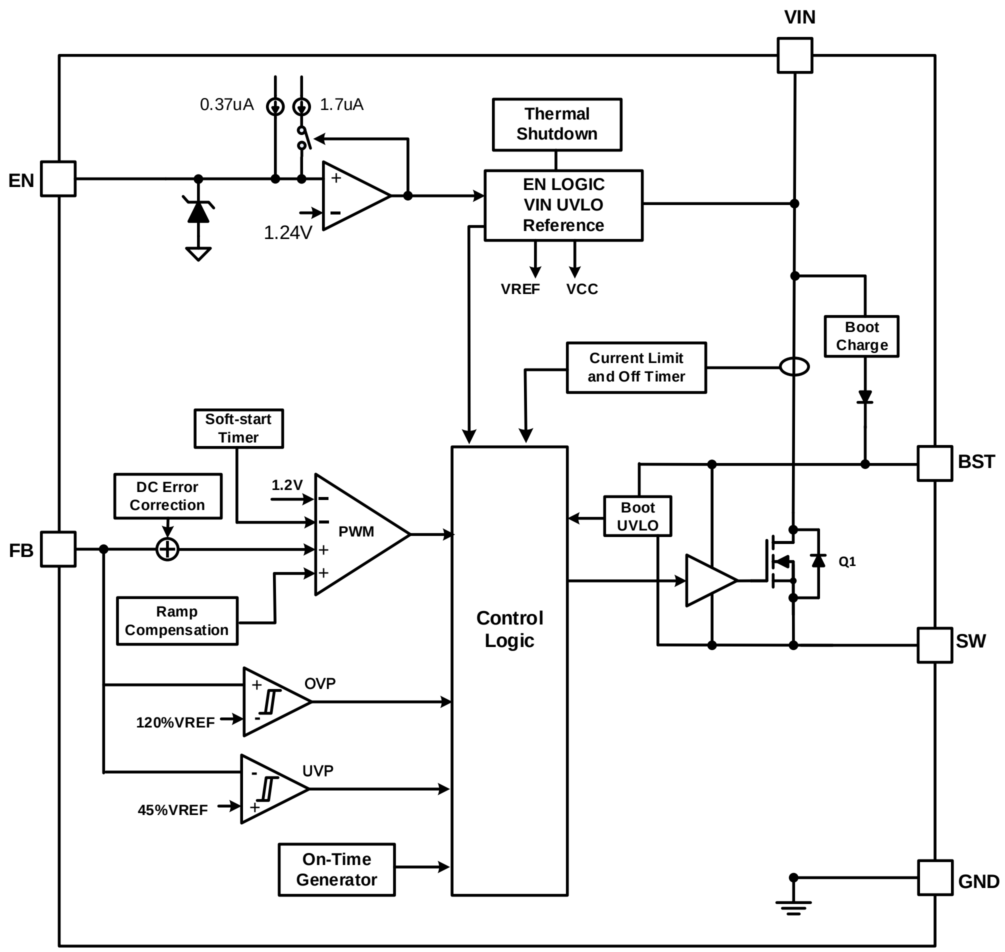

Figure 22-1 Internal Functional Block Diagram

23 Special IO Multiplexing

Precautions for LKS03x special IO multiplexing

The SWD protocol consists of two signal lines: SWCLK and SWDIO. The former is a timer signal that, for the chip, is the input state and does not change the input state. The latter is a data signal that switches between an input state and an output state during data transmission for the chip, which defaults to the input state.

LKS03x can realize the function of multiplexing two IOs of SWD into other IOs. IO multiplexed by SWCLK is P1.8, and IO multiplexed by SWDIO is P1.9. The precautions are as follows:

- Multiplexing is disabled by default, and software is needed to write a 0 to SYS_IO_CFG[6] to enable the multiplexing. That is, after the hard reset of the chip is complete, the initial state is for SWD. The two IOs of the SWD have a pull-up inside the chip (the pull-up resistance of the chip is about 10K). When IO functions as SWD, the pull-up is turned on by default and cannot be turned off. When IO functions as GPIO, pull-up can be worked via GPIO1_PUE[8] and GPIO1_PUE[9]. P1.8 and P1.9 are fixed as SWD functions within 30ms of chip power-on reset, the software can write 0 to SYS_IO_CFG[6], but IO function switching takes effect after 30ms. LRC counting was used for 30ms with some deviation due to process reasons.
- When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.
- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Secondly, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWDIO in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

In the packaging of SSOP24, QFN40, and SOP16L, SWDIO, SWCLK may have bonded with other IOs. At this point, it should be noted that other IO action may cause the chip to misinterpret the SWD action.

The considerations for SWCLK multiplexing are as follows:

- Multiplexing is disabled by default, and software is needed to enable the multiplexing. That is, after the hard reset of the chip, the initial state is used for SWCLK, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 10K). Please pay attention if the initial level is required by the application.
- When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.

- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Second, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWCLK in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

If only SWCLK is multiplexed and SWDIO is not multiplexed at this point, please refer to the above precautions.

RSTN signal is used for external reset pins for the LKS05x chip by default.

LKS03x can realize the functions of RSTN multiplexing into other IO. The multiplexed IO is P0.2. The precautions are as follows:

- Multiplexing is disabled by default, and software is needed to write a 1 to SYS_IO_CFG[5] to multiplex RSTN as a normal GPIO. That is, the initial state of the chip is used for RSTN, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 100K). Please pay attention if the initial level is required by the application.
- The default state is RSTN. Program execution can only be started after RSTN is released normally. The application needs to ensure that RSTN has adequate protection, such as peripheral circuit pull-up. If capacitance can be added, it is better.
- When multiplexing is enabled, the RSTN function becomes invalid. If a hard reset of the chip is required, the source can only be powered down/watchdog.
- RSTN multiplexing does not affect the use of KEIL.

24 Ordering Information

Tray Package:

Package Type	Quantity per disc/tube	Quantity in box	Quantity in case
SOP16/ESOP16L	3000/ disc	6000PCS	48000PCS
SSOP24	4000/ disc	8000PCS	64000PCS
SSOP24	50/ pipe	10000PCS	4000/100000PCS
QFN 8*8	260/ disc	2600PCS	15600PCS
QFN 4*4/5*5/6*6	490/ disc	4900PCS	29400PCS
QFN 3*3	5000/ disc	5000PCS	40000PCS
LQFP48/TQFP48 0707	250/ disc	2500PCS	15000PCS
LQFP64 1010	160/ disc	1600PCS	9600PCS
LQFP100 1414	90/ disc	900PCS	5400PCS
TSSOP20/28	4000/ disc	8000PCS	64000PCS

Reel Package:

Package Type		Quantity per disc/tube	Quantity per box	Quantity boxes per case	Quantity per case
Braid -13 inches	SOP/ESOP8	4000	8000	8	64000
Braid -13 inches	SOP/ESOP16	3000	6000	8	48000
Braid -13 inches	SSOP24	4000	8000	8	64000
Braid -13 inches	TSSOP20	4000	8000	8	64000
Braid -13 inches	D/QFN3*3	5000	10000	8	80000
Braid -13 inches	D/QFN4*4	5000	10000	8	80000
Braid -13 inches	D/QFN5*5	5000	10000	8	80000
Pipe	SOP16	50	10000	10	100000
Pipe	SOP14/SSOP24	50	10000	10	100000
Pipe	TSSOP24	54	6480	6	38880

25 Version History

Table 25-1 Document Version History

Time	Version No.	Description
07/31/2025	2.88	Supplementary SDA Pin Multiplexing
07/22/2025	2.87	Delete the Flash section: and simultaneous erasing of and write-in to one Sector can be made while reading and accessing another Sector
07/21/2025	2.86	Delete the description of the PVD module
07/09/2025	2.85	Grid Module G8 Electrical Parameter Update
06/11/2025	2.84	Added description for floating voltage parameter of grid module G6
05/13/2025	2.83	Delete the component parameters in the recommended circuit block diagram in the pre-drive chapter Added a description of the difference between different versions of the DAC range.
04/27/2025	2.81	Modify the soldering point position of LKS32MC034F2LF6Q8C
04/16/2025	2.80	Add LKS32MC0342FLK608C to the selection table
02/27/2025	2.79	LKS32MC034S2F6Q8B (C) Pin Distribution Correction
01/16/2024	2.78	Add Comparator flip voltage
11/21/2024	2.77	Description of Added ADC Saturation Range
11/12/2024	2.76	Add 034F2LF6Q8C,034F2LM6Q8C,034FLNK6Q8C,034F2LNK6Q8C Add gate drive module G8
09/12/2024	2.75	Add 0342FLK6Q8C Add a description of the GND on the belly of the die
08/19/2024	2.74	Add pre-drive internal connection diagram
08/04/2024	2.73	Order package information updates to confirm package information by package type and package form
07/17/2024	2.72	Increase GPIO High Toggle Threshold
07/05/2024	2.71	Added description for gate drive module G5
07/04/2024	2.70	Update the operating temperature of MCU and driver module
06/04/2024	2.69	034FLK VEM Pin Description Update, Driver Module G6 Parameter Update, 034S2
05/29/2024	2.68	Added internal block diagram of gate drive module G6, and updated electrical parameters of G6
05/07/2024	2.67	034FLK6Q8C Pin Assignment Diagram Modified
04/10/2024	2.66	DAC description update, QFN40L package dimension A size modified
04/01/2024	2.65	Add LKS32MC034FLK6Q8C, DAC adds description of software correction
03/20/2024	2.64	DAC added C version 1.2V range instructions
03/13/2024	2.63	Add C version description
02/27/2024	2.62	Grid drive module G6 parameter update
02/20/2024	2.61	ESD data update
01/19/2024	2.60	Correct electrical performance parameters of grid driver module G6

11/09/2023	2.59	OPA OFFSET Adds the description,Renewal storage temperature
9/25/2023	2.58	Modified Pin temperature
7/24/2023	2.57	Add 034S2F6Q8B
7/28/2023	2.56	Add 038LY6Q8B
7/26/2023	2.55	Add DAC 1.2V range
7/21/2023	2.54	Added 034FL EN pin supplementary description
7/12/2023	2.53	Add the 034FL pin specification
7/6/2023	2.52	Revise the 034FL Pre-drive power supply range
7/5/2023	2.51	Add 038K
6/4/2023	2.5	Add 034FL
4/11/2023	2.49	Modify package name
4/3/2023	2.48	Add CIN detection input filter time
3/24/2023	2.47	Update QFN40(034D/034DO/034S) package dimensions
3/16/2023	2.46	Revise bits of data of UART
1/30/2023	2.45	Revise the description of pins 10 and 35 of 031KL
1/12/2023	2.44	Add characteristic of common mode voltage
1/9/2023	2.43	Add ordering information
12/30/2022	2.42	Revise the 031KL Pin Assignment Diagram
12/29/2022	2.41	Revise the description of the 31st pin of 031KL
12/18/2022	2.4	Add 031KL
12/12/2022	2.36	Revise 5V LDO output characteristic curve
11/28/2022	2.35	Update the LRC clock frequency
11/21/2022	2.34	Update device selection table
11/12/2022	2.33	Update the LRC clock frequency and full temperature error range
11/7/2022	2.32	Add connection resistance between IO and internal analog circuit
10/28/2022	2.31	Add instructions for reading SYS_AFE_INFO to view chip version
10/25/2022	2.3	Revise name of version A/B
10/24/2022	2.2	Revise power supply and add 039D/039PL5/039PL3
10/12/2022	2.14	Add description of MCPWM_SWAP register
9/23/2022	2.13	Revise DateCode format
9/21/2022	2.12	Revise 034DO Pin 8 description
9/16/2022	2.11	034S has LDO inside.
9/6/2022	2.1	Add instructions of version A/B
8/11/2022	2.0	Split 3P3N, 6N and MCU model DS
7/27/2022	1.91	Add 034S
7/21/2022	1.9	Rollback ADC_CH6/7 pin position revision, the second revision time is tentatively scheduled for 2022.10
6/2/2022	1.8	Adjust ADC_CH6/7 Pin location, correct pin multiplexing table. DAC range is changed from 3.0V to 4.8V
3/8/2022	1.7	Add 034D
2/28/2022	1.6	Add 037Q
2/22/2022	1.5	Revise ADC channel number and CMP channel number, remove ADC_CH8 in pin function

1/24/2022	1.4	Revise P0.4, P0.6 Comparator 0 positive input number; Add P0.8 for 033
11/9/2021	1.3	Add 038
11/3/2021	1.2	Add 033, 037F
9/7/2021	1.1	Revised description for VCC power section
9/2/2021	1.0	Initial version

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